Designing SoCs with Planar Fully Depleted Devices and FinFETs

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20nm: End of the Line for Bulk

- Barring something close to a miracle, 20nm will be the last bulk node
  - Conventional MOSFET limits have been reached
  - Too much leakage for too little performance gain

- Bulk replacement candidates
  - Short term:
    - Planar FDSOI or FinFET/Tri-gate/Multi-gate
    - Longer term: III-V devices, GAA, nanowires, etc.

- Rules of the game
  - We’ll look at 20nm and beyond
    - 28nm FDSOI is interesting in its own right, but should be compared with bulk - no commercial 28nm FinFET processes
It’s all about Moore’s Law

<table>
<thead>
<tr>
<th>Product</th>
<th>Customer Expectation</th>
<th>Technology</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nintendo GameBoy (1989)</td>
<td>![GameBoy Image]</td>
<td>CPU: 8-bit Z-80 processor, 1.05 MHz Screen: 2.6&quot; 160 x 144 LCD 4 b/w Connectivity: 4 players by serial cable</td>
<td>$169</td>
</tr>
<tr>
<td>Nintendo 3DS (2012)</td>
<td>![3DS Image]</td>
<td>CPU: Dual core ARM11 MPCore, &gt;500MHz Screen: 800x240 3D plus 320x240, 2GB Flash, AAC audio, 3 cameras, still + 3D video Connectivity: Wifi, browser, shopping</td>
<td>$199</td>
</tr>
</tbody>
</table>

>1000x performance for the same price
Bulk Scaling Challenges

Classic scaling stopped at 90nm

- Beyond that, it’s all about innovation
- Scaling is uneven: some shapes do not scale, others not as much as expected

Beyond that, all about innovation

Consumer expectations set

- Faster, more features, same or lower price

SoC specifications based on consumer expectations

<table>
<thead>
<tr>
<th>Parameter (scale factor = a)</th>
<th>Classic Scaling</th>
<th>Current Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>1/a</td>
<td>1/a</td>
</tr>
<tr>
<td>Voltage</td>
<td>1/a</td>
<td>1</td>
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<tr>
<td>Current</td>
<td>1/a</td>
<td>1/a</td>
</tr>
<tr>
<td>Capacitance</td>
<td>1/a</td>
<td>&gt;1/a</td>
</tr>
<tr>
<td>Power/Circuit</td>
<td>1/a²</td>
<td>1/a</td>
</tr>
<tr>
<td>Power Density</td>
<td>1</td>
<td>a</td>
</tr>
<tr>
<td>Delay/Circuit</td>
<td>1/a</td>
<td>~1 *</td>
</tr>
</tbody>
</table>
## The “Dark Silicon” Problem

<table>
<thead>
<tr>
<th>Node</th>
<th>45nm</th>
<th>20nm</th>
<th>10nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>2009</td>
<td>2013</td>
<td>2017</td>
</tr>
<tr>
<td>Area</td>
<td>1</td>
<td>~1/4</td>
<td>~1/16</td>
</tr>
<tr>
<td>Peak freq</td>
<td>1</td>
<td>1.6</td>
<td>2.4</td>
</tr>
<tr>
<td>Power @ 45nm freq</td>
<td>1</td>
<td>0.6</td>
<td>0.3</td>
</tr>
<tr>
<td>Power @ peak freq</td>
<td>1</td>
<td>1</td>
<td>0.6</td>
</tr>
</tbody>
</table>

### Exploitable Si (equivalent Power)

- 24%
- 10%

**Note:** Precise scaling details don’t matter as much as the general observation.
Getting Beyond Bulk: The Contenders

- FDSOI
  - Fabs: ST, Global, IBM
  - Claim to fame: Better than bulk, easier than fins

- FinFET
  - Fabs: Intel, Global, IBM, Samsung, TSMC
  - Claim to fame: 3D is the future, and the future is now
Ground Rules

- We will compare FDSOI and FinFET on a variety of criteria for a hypothetical new SoC design in a sub-20nm process
  - Standard disclaimers apply (e.g. I am completely ignoring commercial considerations)
- I’ve scored them, based on my opinion (not necessarily the official position of ARM)
- Audience will also vote
- Compare results at the end
Metal Stack

- The same for both
- This matters, because wires are a significant performance limiter
- Advantage: Neither

**FDSOI: 0 points**  
**FinFET: 0 points**
Design Methodology

- Standard SoC design flow
  - Above the standard cell level, there’s nothing special about either FDSOI or FinFETs. Both will have similar look and feel to bulk.
  - This is not quite true for power management, but we’ll talk more about that coming up…
  - Advantage: Neither (actually both)

FDSOI: 0 points  
FinFET: 0 points
Leakage Mitigation

- Back gate bias possible in FDSOI
  - Design challenge, dangerous stray voltages
- Dual gate control possible in FinFET
  - But not really (layout problems), reality is wrap-around gate
- "Wimpy" devices – longer gate lengths possible
  - Theoretically benefits FDSOI more, but limited by ability to build gates
- Doped channel
  - Causes trouble, but possible
- Advantage: Very slightly FDSOI. Both better than bulk

FDSOI: 1 point  FinFET: 0 points
Dynamic Power Mitigation

- Voltage scaling probably better with FinFET
  - Lower performance roll-off than FDSOI
- Minimum size device burns more power for FinFET than FDSOI
  - This is an issue for lower performance parts of SoC
- Advantage: FinFET (2 points)
Supply Chain

- Bulk wafers come from anywhere
- SOI wafers mainly come from SOITEC
- This picture is improving with recent license announcements, so this distinction may disappear over time
- Advantage: FinFET (1 point)
Density

- 3D factor gives fins more drive in a fixed space for fins
- Contacting fins is a challenge, eating area in center of cells
- “Gear ratio” limits usable track heights for fin-based cells
  - Cell height needs to be integer combination of metal tracks, fin pitches
- In practice, smallest cell height is probably the same
- Advantage: FinFET (slight, 1 point)

FDSOI: 1 point

FinFET: 4 points
Manufacturability

- SOI in production for many years
  - FDSOI not dramatically different
  - Already in production at 28nm
- FinFETs have been in high volume production for < 1 year at 1 company
  - And it took them a long time to get there
  - But they got there
- “Bandwagon effect” favors fins
  - You need an equipment supply chain to build a process
- Advantage: FDSOI (slight, 1 point)

**FDSOI: 2 points**

**FinFET: 4 points**
Variability

- Greatly reduced doping leads to lower random dopant fluctuation, lower local variability
- 3D physical structures lead to new forms of variability
- Parasitic variability probably worse for fins
- Advantage: FDSOI (1 point)
Performance

- 3D factor gives increased channel width in fixed area
  - Mitigated somewhat by parasitics
- Discrete device sizing causes some challenges for some specific design-level performance enhancers
  - Beta ratios
  - Staged buffers
- Performance is most important when combined with low voltage operation
  - Iso-performance at lower power
- Advantage: FinFET (2 points)

FDSOI: 3 points

FinFET: 6 points
Design Portability

- In theory, can transfer layout from a bulk process to an FDSOI process at the same fab
  - But I doubt it.
- Could also do the same with FinFET
  - GLOBALFOUNDRIES reports significant commonality in rules
- Can’t port schematics directly to FinFET
  - Device discretization
- Advantage: FDSOI, but it’s slight, 1 point

FDSOI: 4 points

FinFET: 6 points
SRAM

- Bit cells limited in a fin world
  - Discrete sizes for PG, PU, PD
  - Need single fin for area scaling
  - Some combinations cost area
    - 3 fin PD cell same area whether PG is 2 or 3 fins
    - Either read or write assist needed in most cases, sometimes both
- FDSOI more flexibility, may be able to avoid some assists
- Advantage: FDSOI (2 points)
Analog

- Thick oxide devices possible in both
- Discretization limits analog circuits
- Most devices are so big that it doesn’t matter much
- Advantage: Neither
Future Scaling

- FinFET structure can continue for a while yet
  - III-V based on fins
  - Future devices also have 3D structure, why not learn now?
- Counter-argument: Fins will eventually be needed, but planar FDSOI provides a low risk two-stage migration path to fins
- Advantage: FinFET (1 point)

FDSOI: 6 points
FinFET: 7 points
## Comparison Summary

<table>
<thead>
<tr>
<th>Comparison</th>
<th>FDSOI</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal stack, design methodology</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leakage mitigation</td>
<td>1</td>
<td>2</td>
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<tr>
<td>Dynamic power mitigation</td>
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<td>2</td>
</tr>
<tr>
<td>Supply chain</td>
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<tr>
<td>Density</td>
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<tr>
<td>Manufacturability</td>
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</tr>
<tr>
<td>Variability</td>
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<tr>
<td>Performance</td>
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<td>2</td>
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<tr>
<td>Design Portability</td>
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<tr>
<td>SRAM</td>
<td>2</td>
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<td>Analog</td>
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<tr>
<td>Future scaling</td>
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</tr>
<tr>
<td><strong>Total</strong></td>
<td>6</td>
<td>7</td>
</tr>
</tbody>
</table>
Audience Vote

- Possibilities
  - You agree with me that both are plausible contenders for the next generation but FinFETs have a slight advantage
  - You give a slight advantage to FDSOI
  - You vote overwhelmingly for FinFETs
  - You vote overwhelmingly for FDSOI