Enabling Substrate Technology for a Large Volume Fully Depleted Standard

February 24, 2012
1. Technology Requirements for FDSOI 28nm and beyond
   – Substrate definition
   – Soitec product roadmap

2. Controlling key elements for Fully depleted planar FDSOI (FD2D) and FinFET (FD3D) substrates using SOI
   – Thickness control
   – Strain top silicon

3. Supply

4. Other SOI applications
Agenda

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4. Other SOI applications
# Fully Depleted SOI Technology for 28nm & 20nm Mobile

## Technology Requirements for the Advanced Consumer Market

<table>
<thead>
<tr>
<th></th>
<th>High-Performance Capable</th>
<th>Low Active Power</th>
<th>Low Standby Power</th>
<th>Design Portability</th>
<th>Manufacturability in Large Volumes</th>
<th>Optimized Final Application Cost</th>
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6th FD Workshop - February 2012
## Fully Depleted SOI Technology for 14nm Mobile

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<td>Disruptive</td>
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</table>
Soitec Fully Depleted Substrates

Traditional Planar bulk

Severe limitations at 28nm and 20nm

End of life

40nm  28nm  20nm  14nm  11nm

First products expected at 28nm

Foundry offering starting at 14nm

Planar Fully-Depleted

Soitec FD-2D

Soitec FD-3D

FinFET
## Typical Substrate Definition

<table>
<thead>
<tr>
<th>Application</th>
<th>Silicon</th>
<th>BOX</th>
<th>Key elements</th>
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<tr>
<td><strong>PDSOI</strong></td>
<td>55 – 90 nm ± 10nm</td>
<td>145 nm ± 10nm</td>
<td>Thickness uniformity is not critical. &lt;100&gt; orientation for top and base</td>
</tr>
<tr>
<td><strong>FD-2D</strong></td>
<td>12 nm ± 0.5 nm</td>
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<td><strong>FD-3D</strong></td>
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### Product roadmap – SOI for Digital

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<tr>
<th>FAMILY</th>
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<td>XUT+</td>
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<td>High Volume Manufacturing (HVM)</td>
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<tr>
<td>FD 2D</td>
<td>UTBOX25</td>
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- **PDSOI devices**: FDSOI devices
- **FDSOI devices**: FinFET devices
Agenda

1. Technology Requirements at 28nm and beyond
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   - Soitec product roadmap

2. Controlling key elements for FD2D and FD3D substrates using Smart Cut™ technology
   - Thickness control
   - Strain top silicon

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4. Other SOI applications
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- **PDSOI devices**
- **FDSOI devices**
- **FinFET devices**
SOI Thickness Uniformity Requirement

- For a top Si layer thickness controlled within +/- 5Å, 6 sigma; all wafers all sites 
  Avt value obtained for short channels is 1.5mV-µm; typical bulk values are ~2.5mV-µm

- Spec for substrate top Si layer is ±5Å uniformity range (all points, all wafers)

![Diagram showing gate length vs. A_Vt](image)

- Extremely low local $V_T$ variation
- Local $T_{Si}$ well controlled < 5Å
- Record and reproducible $A_{VT} = 1.25$ mV.µm @ Lg=25nm

K. Cheng, A. Khakifirooz et. al. IEDM 2009
Smart Cut™ Process Sketch for UTBOX25: *Uniformity Control @ Atomic level*

**Donor Wafer**
- Buried Oxide Growth
- Implantation

**Handle Wafer**
- Cleaning & Bonding

**UTBOX25**
- SOI Layer
- BOX Layer
- Si Substrate

**SmartCut Splitting**

**Recycling**
- SOI Wafer
- Smoothing & Finishing

Thickness Uniformity Driver
Smart Cut™ process enables Å Uniformity

1. Thermal Oxidation ➞ Excellent within wafer (WiW) uniformity
2. Hydrogen implant ➞ Very uniform Rp control
3. Smart Cut tuning ➞ Post splitting range ≤ oxide range
4. Surface smoothing
5. Wafer to Wafer (WtW) thickness fine tuning

SOI Thickness Range @ 3.13 Å

WiW thickness range after oxidation

6 sigma
APC Strategy in Final Thinning:

**Wafer to Wafer uniformity <±5Å**

**Wafer-to-wafer control managed thru APC strategy**

**Finishing process flow description**

- Sacrificial oxidation
- Thickness measurement
- Cleaning #1
- Cleaning #N
- Final sorting
- Final thickness fine adjustment

**Process step**

- **Fully automated dynamic processing**

**SOI Thickness control <±15 Å by line tool to tool matching**

**Wafer to wafer < ±5 Å**
All points, All wafers Uniformity

SOI Mean Thickness (Å)

Quarter 2010-Q2 2010-Q3 2010-Q4 2011-Q1

Total SOI Thickness fluctuation (Å)

Quarter 2010-Q2 2010-Q3 2010-Q4 2011-Q1 2001-Q4

Maximum
Minimum

+/- 5 Å
+/- 10 Å
SOI Thickness Control: All Points, All Wafers

Wafer to Wafer uniformity <±5Å

UTBOX25 WiW Range 3.13 Å
SOI Thickness Variation contributions

Thickness control is ensured for all spatial frequencies
Product roadmap – SOI for Digital

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PDSOI devices  FDSOI devices  FinFET devices
Integrating Performance in SOI: sSOI

- **Donor Wafer**
  - SiGe Buffer layer Epitaxy
  - sSi layer Epitaxy
  - Implantation
  - Cleaning & Bonding

- **Handle Wafer**
  - Buried Oxide Growth

- **sSOI – BOX25**

  - sSOI Layer
  - BOX Layer
  - Si Substrate

- **SmartCut Splitting**

- **Recycling**
  - sSOI Wafer
  - Selective Etching & Finishing

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sSOI Raman Strain Mapping: 
*Performance booster*

Wafer map showing the uniformity of tensile strain across the wafer

Demonstrated Strain > 1300 MPa with less than 10% variation
Product roadmap – SOI for Digital

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- PDSOI devices
- FDSOI devices
- FinFET devices
Fully Depleted 3D substrates: Faster, Cheaper, Better

1. Development Lead Time
   - SOI-based Isolation is much simpler

2. Cost and Cycle time for FinFET
   - SOI-based Isolation goes directly into fin module and device integration

Process & statistical variability
- Process induced fin height variability
- Implant induced RDF

Bulk-based Isolation adds several key modules
- N-P Trench Isolation Module
- Oxide deposition / Oxide etch / CMP
- Nwell lithography / pFET isolation doping
- Pwell lithography / nFET isolation doping

SOI FinFET is compelling on Key Fronts

FD 3D Susbstrate
- No fin height variability
- No RDF
- Simplest Fin formation
- Shorter cycle times
- Significant Cost savings

Bulk
- Implants Topi
- STI
- Oxide Recess
- Transistor
- BEOL

FD 3D Substrate
- Si etch
- Transistor
- BEOL

Time to Market
FinFET: Thickness uniformity for Fin height control

Wafer map of top Si layer thickness:
Total range all sites ±3Å

Fin height definition is done by tuning the top Si thickness

Target thickness variation +/- 10Å
## FD-2D and FD-3D substrates technical readiness

<table>
<thead>
<tr>
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<th>BOX</th>
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<th>Status</th>
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2. BOX thickness key for back bias  
3. Cristal orientation to boost mobility  
4. Strain top silicon to boost performance | ✓ +/- 5A thickness control implemented  
✓ 10-25nm available  
✓ <100> <110> notch orientation  
✓ sSOi sample available |
| FD-3D | 30 nm ± 2nm | 50 - 145 nm ± 5nm | 1. Thickness uniformity drives Fin height control  
2. BOX thickness to be optimized  
3. Cristal orientation open  
4. Strain top silicon to boost performance | ✓ +/- 10A thickness control implemented  
✓ Collaboration with cust  
✓ <100> <110> notch orientation  
✓ First sample Q2CY12 |
Agenda

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FD-2D / FD-3D Opportunities

Depending on adoption up to 6 millions SOI wafers needed in CY17

Wafer Demand per node:

- 16nm IDM
- 22nm IDM
- 32nm IDM
- 16/14nm Foundries
- 22/20nm Foundries
- 32/28nm Foundries

Scenario:
Early Transition to 14nm
2 years from 28nm to 20nm (hvm),
2 years from 20nm to 14nm (hvm)

Forecasted wafer demand

Estimates based on IC Insights, Semico, and Gartner forecast analysis.
Current Model: Soitec Manufacturing & Licensing

Customer
IDM/Foundries

Additional Licensees

ShinEtsu
Soitec
Smart Cut™ like sources

Current suppliers

New Licensees Investment

SOI Fab, Bernin (France)

SOI Fab, Singapore

Fast ramp to 6-7 Mwfr/yr when needed

1M wfr/yr

2 M wfr/yr

5 M wfr/yr

6-7 M wfr/yr

9 months

9 months

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Ultrathin Body and Box SOI material is ready to support FD devices adoption from 28nm node

✓ HVM roadmap in place & readiness at 28nm node

✓ 20nm node specifications achieved

✓ Technology booster planned in roadmap

✓ Smart Cut is high volume proven standard
   ➢ 2 suppliers to support volumes up to 2014 & industrial model demonstrated
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A wide offer of materials for a broad range of applications

<table>
<thead>
<tr>
<th>MARKETS</th>
<th>Computing &amp; Telecommunications</th>
<th>Consumer &amp; Mobile</th>
<th>Industrial &amp; Automotive</th>
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<td><strong>APPLICATIONS</strong></td>
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**Soitec products**
- Xtreme SOI Premium SOI
- Wave SOI GaAs EPI RF SOS
- Smart Power SOI
- Imager SOI Stacking for Imager
- Smart Power SOI
- Photonics SOI Stacking for MEMS
SOI Product Lines

- **Imager SOI**
  - 1.5µm
- **Smart Power SOI**
  - 1.0µm
  - 2.0µm
  - 3.0µm
- **Photonics SOI**
  - 0.1µm
  - 0.145µm
  - 0.05µm
- **Wave SOI**
  - 0.01µm
  - 0.01µm
  - 0.03µm
  - 0.07µm
  - 0.25µm
- **Premium SOI**
  - 0.09µm
- **FD2D/FD3D**
  - 0.03µm
  - 0.01µm

Buried Oxide (BOx), ‘Base’ or ‘handle’ = ‘Bulk substrate’

BOX Thickness

Top Si Thickness

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Thank You!
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