Designing with FD-SOI – Benefits and Challenges

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Corporate Overview

- Founded in 2003
- Global Engineering / Support Centers
  - Flexible design models from traditional ASICs to complete turnkey IC development
  - 79% Engineering
- World leader in ASIC design and manufacturing
  - Technologies from 0.35um to 14nm
  - ISO9001:2008 registered

Our Mission

Enhance the value of customers’ products by innovating at every stage of design — system, architecture, functional logic, physical and software — to deliver fully tested silicon and platforms
One Stop Shop for ALL ASIC needs

Innovating on top of open-business-model

Front End Solutions & Services
- Full turnkey solutions – Spec2Parts
- Spec2Boot Platform
- Front-end Design, Software & Validation
- Virtual Prototyping

Software and System solutions

Technology Centers of Excellence & Innovation
- Dedicated ARM Hardening Team
- 28G Semtech SerDes Testchip in 28nm
- First to demonstrate 2.5D Silicon and Package

Evaluation Platforms Key to Complex IP Integration

Back End Solutions & Services
- Physical Design from 130nm to 14nm
- OpenModel IP from best in class IP Partners
- Advanced packaging Capability
- Robust Test Methodologies & qualifications

Foundation Technology and IP

Extend Offering with talented teams
Open-Silicon Innovation
Standard Open Business Model + Execution

A leader in Semiconductor Solutions
Open-Silicon Achievements

- 90+ million parts have shipped with 30 DPPM
  - 7 foundries, 30+ process technologies, 40+ IP vendors
- 300 Designs in about 100 different end applications
  - Networking, telecom, storage, computing, consumer, industrial & wireless
- Over 150 unique customers from tier-1 system companies to startups
  - NA, Japan, EU, Israel, China, Korea, rest of APAC and India
- 68% of customers came back to Open-Silicon for next design
  - 15% of customers have done 3+ ASICs with Open-Silicon
ST-28nm FDSOI PD Experience
Open-Silicon and FD-SOI

- Open-Silicon has been engaging with STMicro since 2013
- We are a channel partner with ST offering the 28-FDSOI process for ASIC solutions in Japan for certain markets and customers.
- Open-Silicon’s OpenMODEL™ enables us to work with multiple fabs
  - Process to **qualify IP**
  - Process to **pipe-clean design-flow** before implementing a customer design
- We have already completed a pipe-clean flow
- We are currently engaged in a test-chip tapeout with a customer using 28-FDSOI
28nm FDSOI Advantages

- Total dielectric isolation
  - Lower Source-Drain capacitances (to ground plane)
  - Better Latch-up immunity

- Around 35% Less Power than bulk CMOS for same frequency based on lower VDD and lower leakage.

- No doping in channel region & presence of isolation layer enables less leakage

- Less performance variation across PVT

- RVT & LVT std cells are available

- Performance / Power adjustable through body biasing – RBB and FBB

Courtesy: ST Microelectronics
LVT Buffer-Delay vs VDD Scaling – Open-Silicon Data

- Poly-bias is used to offer increased richness in libs
  - More options than standard multi-channel
- 4 options P0, P4, P10 and P16
  - P0 faster, but leakier than P16
- Compared to CMOS lower PVT variation in timing (35, 38, 44ps)
  - Benefit
- At lower voltages the variation in timing larger - Challenge
**ST28nmFDSOI Benefits and Challenges**

- **RVT and LVT - Challenge**
  - Cells cannot be mixed in the same PNR block (Nwell structure gets flipped for diff VT)
  - Across different blocks using RVT and LVT is OK

- **STM std. cells are designed for low power implementation compared to super high performance – Challenge and Benefit**
  - Higher performance requires higher voltage or FBB – increases power.
  - Reverse Body Bias can further lower power, with some reduction in frequency.
  - Reverse/Forward Body Bias requires additional power/gnd mesh to be implemented in the layout.

- **STM std. cells support wide range of VDD – 0.6v (Slow) to 1.3v (Fast) - Benefit**
  - Fine adjustment of power vs frequency, libs using 0.05v increment libs are available
  - Memories support dual rail capabilities
  - To reduce design complexity VDD-of-IP = VDD-of-StdCell = VDD-of-SRAM
    - Less VDD supplies, easier design
ST28nmFDSOI Benefits and Challenges

- MBIST insertion flow from STM uses Atrenta SpyGlass DFT tool - Comment
  - Master and Slave controllers are the same size as other industry standard mBIST implementations
- EMET structures – Challenge and Benefit
  - Many Special Cells are needed – so layout of these cells adds complexity
  - These cells help reduce process dispersion and potentially improve yield
- Antenna DRC checks are needed to protect Gates and Source/Drain – Challenge (small one)
  - In bulk CMOS antenna DRC checks are needed only to protect the Gates from dielectric breakdown
  - In FDSOI there is insulation layer at the Source/Drain, hence Source/Drain should also be protected
  - In most cases the PnR tools were able to fix these issues
- Ultra-Low-k dielectric, between metals – Benefit
  - Ensures lower net cap, improve speed and reduce switching power
- IO are PVT compensated – Benefit
  - Slew and transition are controlled, but extra work to manage the PVT compensation circuit
- Current STM FDSOI implementation supports only FlipChip IO – Challenge
GPU Core – pipe-clean flow

- Die size: 2.419mm X 2.219mm
- Area: 5.368sq.mm
- 3.2 Million std cell instances
- Hierarchical block
- 4 instances of ‘sp_pipe’ sub-blocks (500K std cells each)
- 3.1W total power @ 666MHz at tt_125C_1v (760mW per sp_pipe instance) without body bias.
- Block taken through full PNR flow including DRC/LVS/DFM checks.

STM EMET structures (equivalent of TSMC TCD / GF TG-stack structures for Fab process control)
## DSP Core (effect of Forward Body Bias – FBB)

### DSP Processor Block

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Block size</strong></td>
<td>1345um x 1200um (area 1.614mm²)</td>
</tr>
<tr>
<td><strong>Std cell count</strong></td>
<td>523,425</td>
</tr>
<tr>
<td><strong>Utilization</strong></td>
<td>78% (postroute)</td>
</tr>
<tr>
<td><strong>No. of metal layers</strong></td>
<td>8</td>
</tr>
<tr>
<td><strong>PVT conditions</strong></td>
<td>SS_0.75v_-40c / TT_0.8v_25c / FF_0.9v_125c</td>
</tr>
<tr>
<td><strong>Total power without FBB</strong></td>
<td>500mW (@ TT_0.9v_125c @ 666MHz)</td>
</tr>
<tr>
<td></td>
<td>Std cell power -- 258mW</td>
</tr>
<tr>
<td></td>
<td>Memory power -- 242mW</td>
</tr>
<tr>
<td><strong>Total power with FBB – 1v</strong></td>
<td>915mW (@ TT_0.9v_125c @ 800MHz)</td>
</tr>
<tr>
<td></td>
<td>Std cell power -- 605mW</td>
</tr>
<tr>
<td></td>
<td>Memory power -- 310mW</td>
</tr>
<tr>
<td><strong>Total Leakage power without FBB</strong></td>
<td>75mW @ TT_0.9v_125c</td>
</tr>
<tr>
<td><strong>Total Leakage power with FBB</strong></td>
<td>331mW @ TT_0.9v_125c</td>
</tr>
</tbody>
</table>
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Start

Synthesis

Insert test structures
-- Tessent/Synopsys MBIST insertion
-- Structures for leakage based binning, biasing
  - Bscan, IP specific test structures

Place and route
-- TG Stack Insertion
-- Multi Vt optimization
-- Multi channel optimization
-- DFM aware routing
-- Power aware Decap insertion

Pre-signoff DFM
-- 28nm Design rules
-- Litho hotspot fix

Timing analysis
-- STA at 8 PVT/RC corners
-- OCV, SI, MMMC

Power analysis
-- Dynamic rail analysis

Tessent/Synopsys MBIST insertion

Structures for leakage based binning, biasing
- Bscan, IP specific test structures

Scan insertion
-- embed test structures

Timing ECO

Timing OK?

Pattern generation
-- transition
-- path delay
-- bridging

Signal EM OK?

Formal verification
-- 28nm DRC/DFM/LVS
-- Sealing Integration

Signal EM analysis
-- VCD pattern based

Simulation

PDV checks
-- 28nm DRC/DFM/LVS
-- Sealring Integration

Timing OK?

All checks OK?

End

Tapeout

Power analysis

28nm Bulk Flow
Start

Synthesis

Insert test structures
  -- Atrenta / ST MBIST insertion Flow
  -- Structures for leakage based binning, biasing
  - Bscan, IP specific test structures

Place and route
  -- EMET structure Insertion
  -- Multi channel (poly-bias) optimization
  -- DFM aware routing
  -- Power aware Decap insertion
  -- Structures for Body-bias support

Pre-signoff DFM
  -- 28nm Design rules
  -- FDSOI specific Rules
  -- Litho hotspot fix

Scan insertion
  -- embed test structures

Power analysis
  -- Dynamic rail analysis

Extraction
  -- 4 RC corners
  -- Variation & CMP aware

Timing analysis
  -- STA at 8 PVT/RC corners
  -- OCV, SI, MMMC

Timing OK?

Signal EM repair file

Pattern generation
  -- transition
  -- path delay
  -- bridging

Simulation

Tapeout

Formal verification
  -- 28nm DRC/DFM/LVS
  -- FDSOI DRC/DFM
  -- Sealring Integration

All checks OK?

Timing ECO

Minor changes from 28nm bulk CMOS to 28nm FDSOI.
Summary

• Ideal for **consumer** and **networking/telecom/storage/compute** applications

• Several design advantages – power, performance and options for libraries
  – Same design flow as for 32/28nm bulk CMOS process
  – Similar design cycle time as 28nm bulk CMOS
  – Industry standard EDA tools used – no custom tools needed

• Open-Silicon has good experience with 28 FD-SOI

• FD-SOI is a good option for Custom ASIC solutions and SOCs