



*SOI TECHNOLOGY:  
SEMICONDUCTOR PERCEPTION &  
AWARENESS STUDY*

*2008 SILICON-ON-INSULATOR SURVEY ANALYSIS*

In Collaboration with:



## EXECUTIVE SUMMARY

### Purpose of the SOI Study

Silicon-on-insulator (SOI) adoption initially began within the integrated device manufacturer (IDM) community in the late 1990s for its high-performance advantages. Since the demand for information on SOI has spiked in growth over the past few years, the Global Semiconductor Alliance (GSA) and the SOI Industry Consortium collaborated in late 2007 to determine industry awareness and the various perceptions of SOI technology. This joint effort resulted in an online survey, which was conducted in April 2008.

Key survey findings include:

- Promising growth potential in SOI technology.
- Significant interest in SOI for low power.
- Counter perceptions that SOI is only applicable at leading-edge nodes.

### Promising Growth Potential

The survey results confirmed promising interest in SOI technology, with 23% of the participants currently using SOI technology. Two-thirds (64%) do not use it today, but are interested in its potential benefits. The main reason for not using SOI and those indicating no interest in its future adoption specified that the *potential cost increase* was the number-one reason they are not interested in adopting SOI technology.

### Power Savings

In particular, 46% of the respondents perceive that power savings is the single-most important advantage of using SOI for their business. Further results indicate that a 30% power savings would motivate 70% of the respondents to invest in an evaluation of SOI.

### Not Just for Leading Edge

Finally, the results of the survey challenged the perception that SOI was only for the most advanced nodes. The majority of the respondents are using 90-nanometer, 130-nanometer or 0.18-micron as their most advanced technology today. The survey results indicated that 72% of the respondents would consider a transition to SOI at 45-nanometer, 65-nanometer or 90-nanometer.

The survey reflected the need for more education and availability of ecosystem deliverables from silicon, IP and EDA suppliers, and that there is a particular need for more SOI libraries at different technology nodes and for more silicon suppliers. The survey confirmed a top agenda item to address is the perception of cost as the top barrier to adoption. The good news from the survey is that 43% of those surveyed are willing to accept 5%-10% additional total cost, including design costs, in return for a 30% power savings. For performance, 33% of those surveyed are willing to accept 5-10% additional total cost in return for a 20% performance gain.

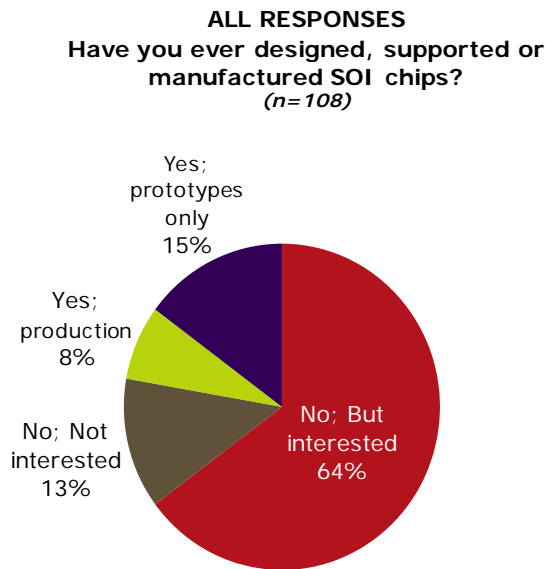
In conclusion, the survey has provided valuable insight into the perceptions and information gaps of a relevant group of designers not currently using SOI, and this initial effort between the GSA and the SOI Industry Consortium is providing a valuable platform for SOI education for their members and paves the way for future collaboration.

**ANALYSIS**

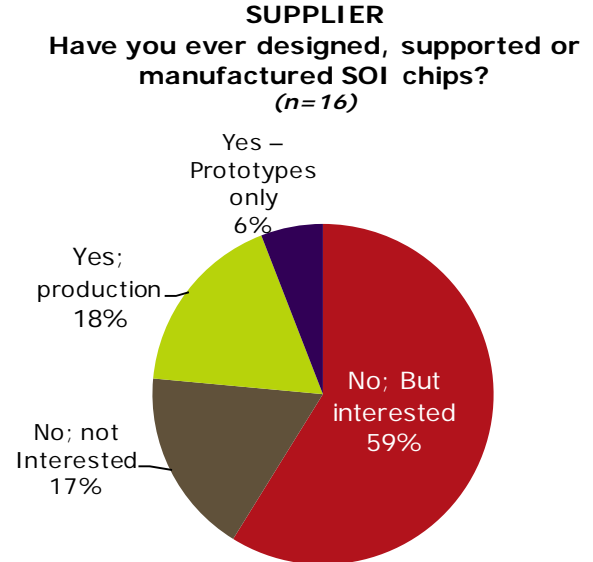
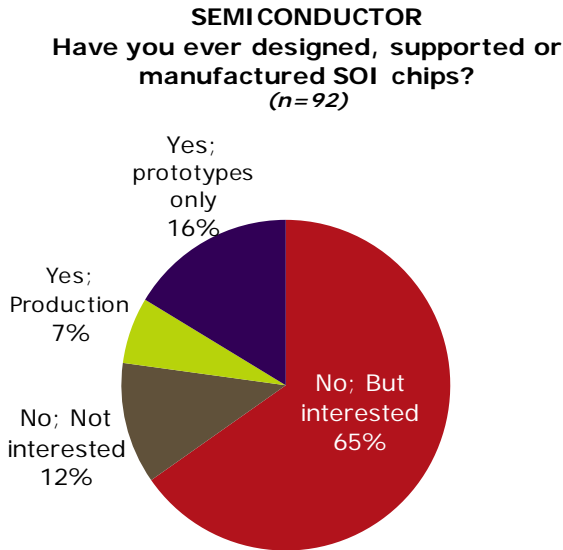
**Strong Interest in SOI from Respondents Due to Perceived Power Savings**

One of the most significant findings is that a large majority of total respondents (71) indicated they are interested in using SOI and have not previously used it. The survey results confirmed a promising interest in SOI with 23% of participants currently using SOI technology and 64% not using it today, but are interested (Figure 1).

When the data is segmented, and the semiconductor companies (92) are separated from the supplier base (16), 23% have either used it in production and/or prototypes, with another 65% demonstrating future interest in the technology (Figure 2). Figure 3 indicates 24% of the suppliers have used SOI and another 59% show future interest.



*Figure 1. Results concluded that 23% of respondents are currently using SOI technology and 64% are interested but have not used it previously.*



Figures 2-3. Results concluded that 23% of semiconductor respondents and 24% of and supplier respondents are currently using SOI technology, and 65% and 59%, respectively are interested, but have not used it previously.

**Biggest Reason Your Company is not Interested in Implementing SOI Technology**  
*(n=108)*

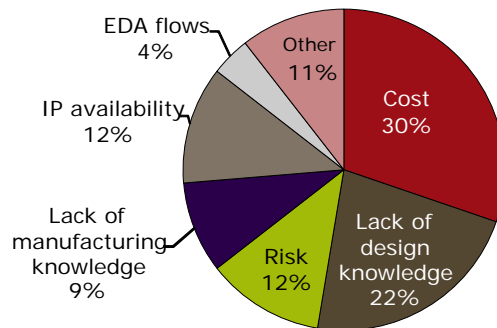


Figure 4. Cost is identified as the number-one reason companies are not interested in implementing SOI technology, followed closely by lack of design knowledge.

Those who are not using SOI and are not interested specified that the potential high cost was their number-one reason they are not interested in adopting SOI technology (Figure 4).

SOI has traditionally had success in segments where high performance matters, such as power-sensitive segments in the consumer category. This goal was accomplished with 29% of all respondents (*n=90* (Note: multiple answers were allowed per category)) involved in consumer product development (Figure 5),

followed by networking and telecom at 24%. For semiconductor companies, 33% are in consumer markets, with 24% in networking & telecom, compared to 24% in networking and telecom, followed by 18% in data processing and 14% in consumer markets for suppliers (Figures 7-8). One of the SOI Consortium's missions is to successfully broaden the markets for SOI innovation.

In addition, 38% of the respondents indicated that their principal design application is digital design and 37% analog/RF design (Figure 6), compared to 41% and 38% in the semiconductor space, and 41% and 31% in the supplier space, respectively (Figures 9-10).

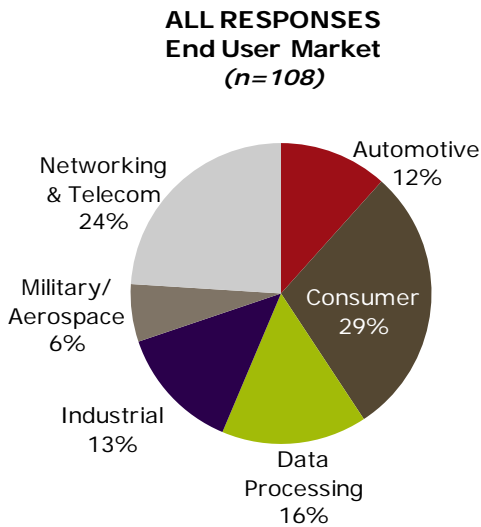


Figure 5. 29% Consumer markets, followed by 24% networking & telecom

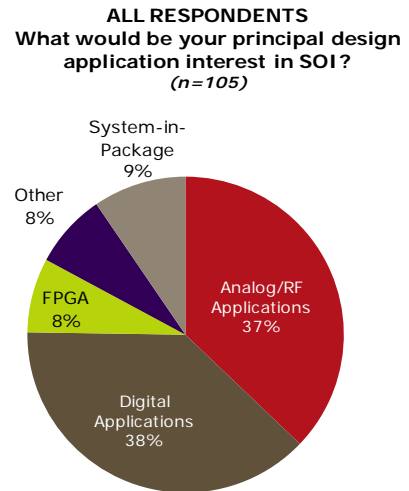


Figure 6. 38% Digital applications, followed by 37% in Analog/RF.

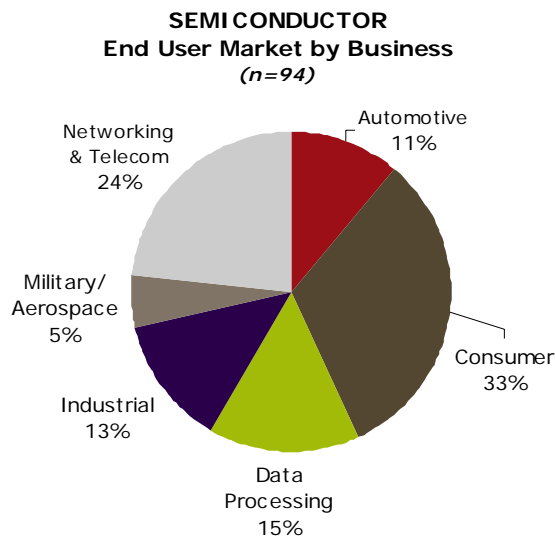


Figure 7. In the Semiconductor arena, 33% are in Consumer markets, with 24% in Networking & Telecom.

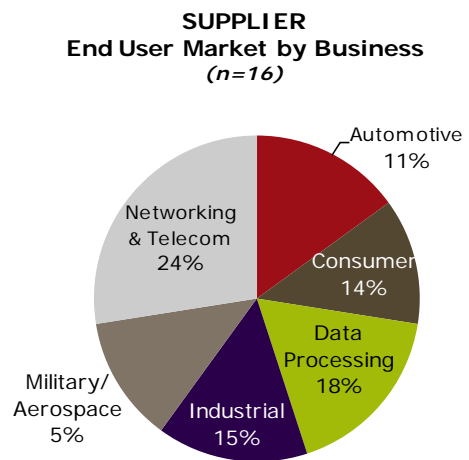


Figure 8. In the Supplier base, 24% are in Networking and Telecom, followed by 17% in Data processing and 13% in Consumer markets.

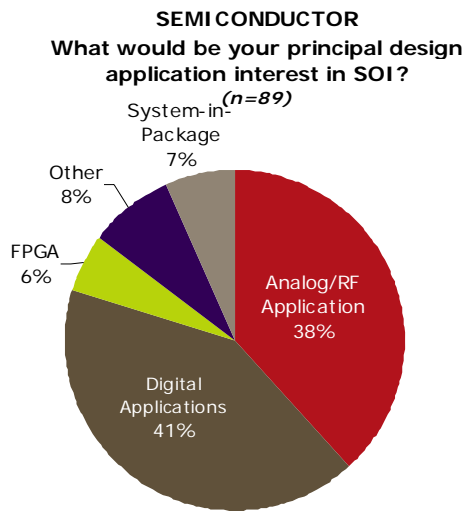


Figure 9. In the Semiconductor space, 41% and 38% indicated their design is principally in the digital and analog/RF spaces, respectively.

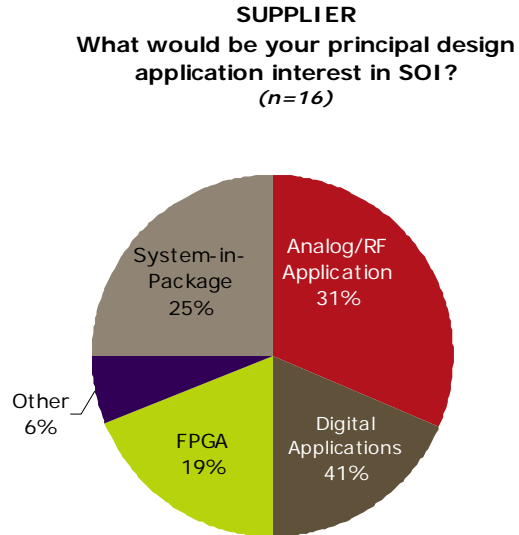


Figure 10. In the Supplier space, 41% and 31% indicated their design is principally in the digital and analog/RF spaces, respectively.

**Power Savings**

The survey responses reflected a strong interest in SOI for power savings. Of all of those responding, 46% indicated that they perceive power savings as the single-biggest potential advantage of using SOI for their business (Figure 11), and 70% of the respondents indicated that 10% to 30% improvement in power savings would motivate them to invest in an evaluation of SOI (Figure 14). When analyzing this against semiconductor companies specifically, the perceived importance of power savings increases to 51% followed by 21% for higher performance (Figure 12). Ironically, only 18% of suppliers accounted for a perceived specific interest in higher performance and 24% for power savings, preferring to lump all perceived benefits as attractive with 52% stating all of the above (Figure 13). Greater reliability was only addressed by semiconductor companies, coming in at a minimal 2% (Figure 12).

And when considering the total product cost of adopting SOI, 43% of the respondents indicated they would be able to incur 5%-10% additional total product cost, including design costs, to achieve a 30% power savings (Figure 17).

**ALL RESPONSES**  
**What are the biggest potential advantages of using SOI for your business?**  
*(n=106)*

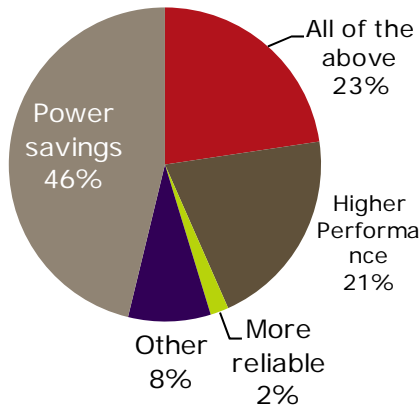
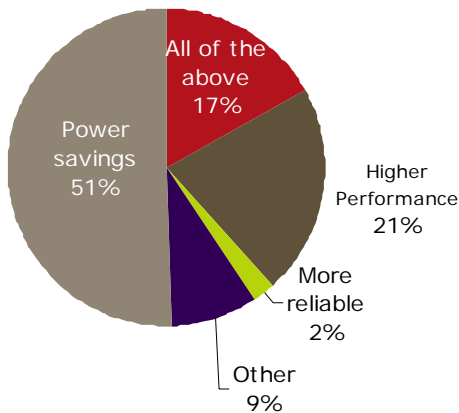
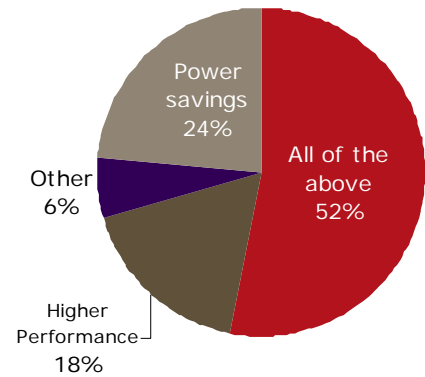


Figure 11. 46% of respondents indicate power savings as the biggest potential advantage for SOI in their business.

**SEMICONDUCTOR**  
**What are the biggest potential advantages of using SOI for your business?**



**SUPPLIER**  
**What are the biggest potential advantages of using SOI for your business?**



Figures 12-13. 51% of semiconductor respondents indicate power savings as the biggest potential advantage for SOI in their business, vs. just 24% of suppliers.

**What demonstrated percentage power savings improvement would motivate you to evaluate SOI?**  
(n=97)

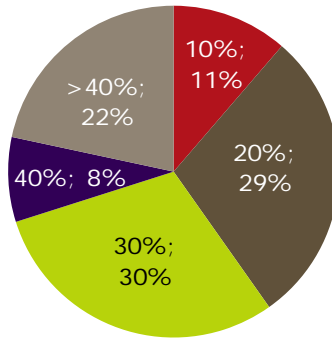
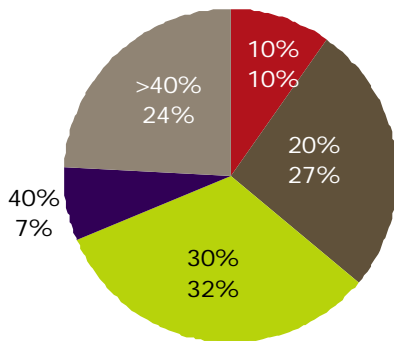


Figure 14. 70% of all respondents indicate 10%-30% power savings would motivate them to evaluate SOI.

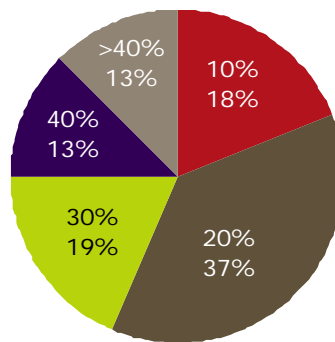
**SEMICONDUCTOR**

**What demonstrated percentage improvement in power savings would (or did) motivate you to invest in an evaluation of SOI?**



**SUPPLIER**

**What demonstrated percentage improvement in power savings would (or did) motivate you to invest in an evaluation of SOI?**



Figures 15-16. 69% of Semiconductor and 74% of all supplier companies indicate 10%-30% power savings would motivate them to evaluate SOI.

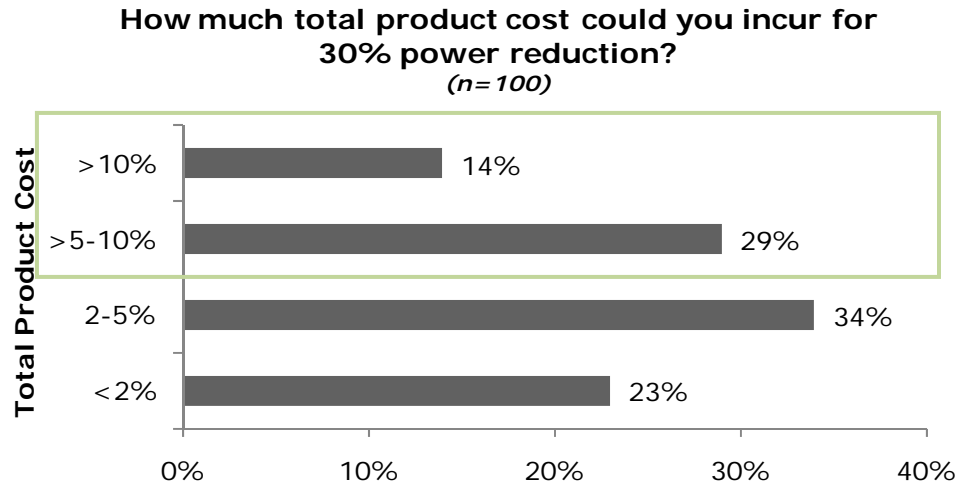
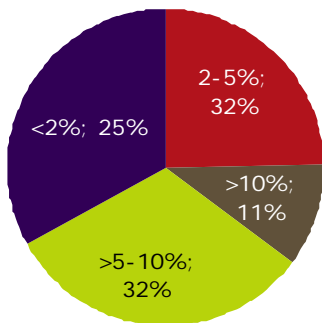
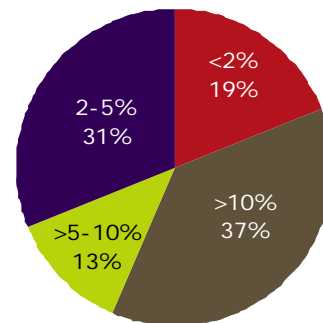


Figure 17. Out of all responses, 43% would incur a >5% total product cost increase for a 30% power reduction in their design.

**SEMICONDUCTOR**  
How much additional total product cost (including design) could you incur for 30% power reduction?



**SUPPLIER**  
How much additional total product cost (including design) could you incur for 30% power reduction?



Figures 18 – 19. 43% of semiconductor respondents and 50% of supplier respondents indicated they could incur >5% total product cost for a 30% power reduction in their design.

While power savings was the single biggest potential advantage, higher performance remains a strong second in importance amongst these respondents. When asked about performance gains that would motivate an SOI evaluation, for a 20% gain in performance, 57% of respondents would evaluate SOI (the sum of respondents at 5%, 10% and 20% gains) (Figure 20). Another result of the survey indicates that for 20% performance gain, 33% would incur 5%-10% additional product cost, including design costs (Figure 23).

**What demonstrated performance gains would motivate you to evaluate SOI?  
(n=99)**

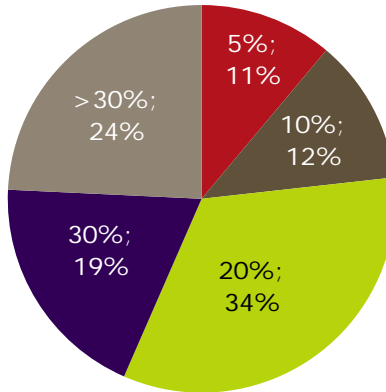
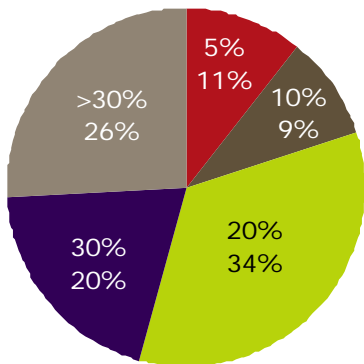


Figure 20. For a 5%, 10% or 20% gain in performance, 57% of respondents would evaluate SOI.

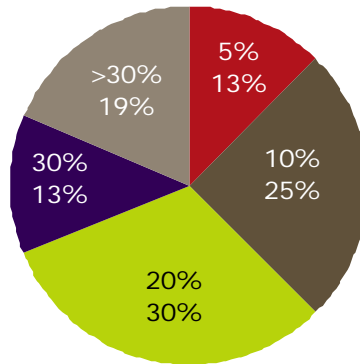
**SEMICONDUCTOR**

**What demonstrated percentage improvement in performance would (or did) motivate you to invest in an evaluation of SOI?**



**SUPPLIER**

**What demonstrated percentage improvement in performance would (or did) motivate you to invest in an evaluation of SOI?**



Figures 21-22. For a 5%, 10% or 20% gain in performance, 54% of semiconductor respondents and 68% of supplier respondents would evaluate SOI.

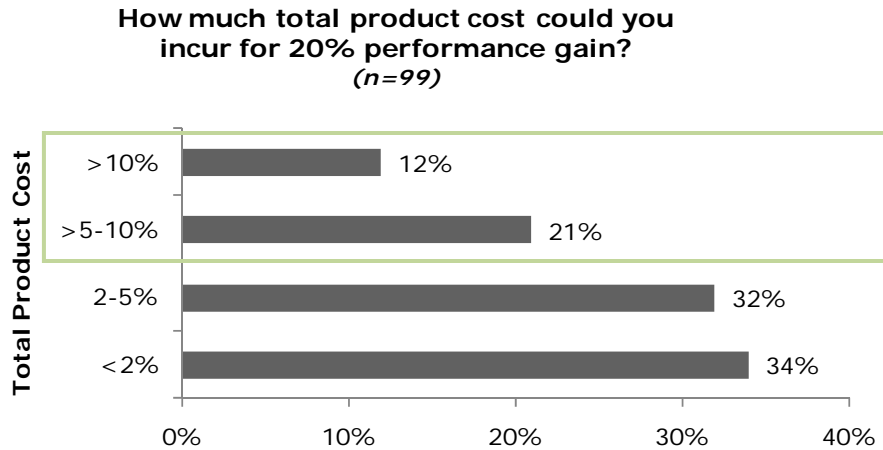
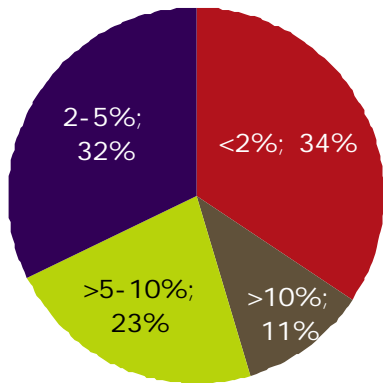
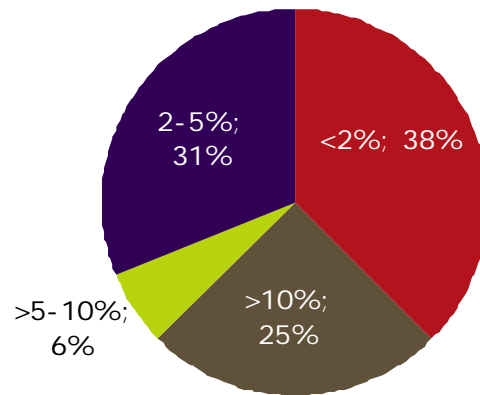


Figure 23. For a 20% performance gain, 33% of all respondents would incur a total product cost of at least 5%-10%.

**SEMICONDUCTOR**  
How much additional total product cost (including design) could you incur for 20% speed improvement?



**SUPPLIER**  
How much additional total product cost (including design) could you incur for 20% speed improvement?



Figures 24-25. For a 20% performance gain, 34% of semiconductor respondents would incur a total product cost of at least 5%-10% and 31% of suppliers would do likewise.

**Survey Confirms Need for More SOI Education and Awareness**

When asked to rank what would benefit them most in evaluating whether to use SOI in their next project, the ranking result was:

1. Power and performance results
2. Cost analysis examples by market segment
3. Silicon validated IP
4. EDA reference flows
5. Success stories
6. Design services

A similar survey question asked what the biggest reason was for not evaluating or using SOI today. In this response, there is little surprise for those working on SOI adoption to see the top reason cited was the perceived additional cost of SOI, followed by lack of design knowledge and then risk and IP availability – each tying for the third-biggest reasons SOI isn't currently evaluated or used (Figure 26).

Number-One Reasons Companies are Not Adopting/Using SOI Technology	Rank
Cost	1
Lack of design knowledge	2
Risk	3*
IP availability	3*
Lack of manufacturing knowledge	5
EDA flows	6
Other	7

Figure 26. Ranked reasons why companies are not adopting/using SOI Technology today (\*Tie)

An encouraging response on cost was given by respondents regarding how much product cost they would incur to achieve 30% power savings (Figure 17). More than 40% of those surveyed are willing to accept at least 5%-10% additional total cost in return for a 30% power savings, a level at which 67% of the respondents felt they capture future market opportunities (Figure 27). When segmented by semiconductor and supplier, 69% of semiconductor respondents and 56% of suppliers believe they can capture a future market opportunity with 10%-30% power savings from SOI (Figures 28-29).

**ALL RESPONSES**  
**What % proven improvement in power savings from SOI would enable you to capture a future market opportunity?**  
 (n=98)

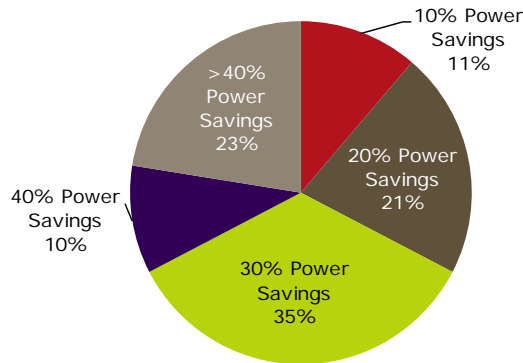
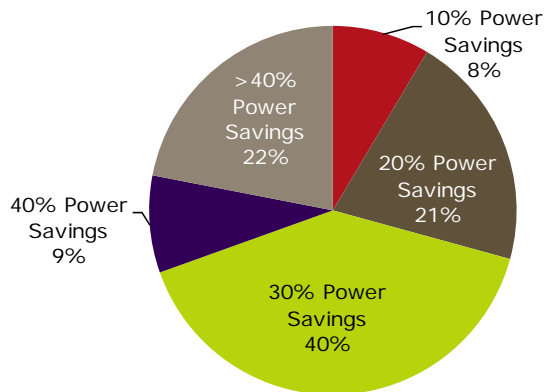
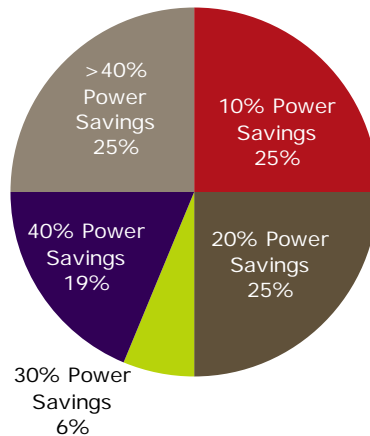


Figure 27. 67% of respondents believe they can capture a future market opportunity with 10%-30% power savings from SOI.

**SEMICONDUCTOR**  
**What % proven improvement in power savings from SOI would enable you to capture a future market opportunity?**  
 (n=82)



**SUPPLIER**  
**What % proven improvement in power savings from SOI would enable you to capture a future market opportunity?**  
 (n=16)



Figures 28-29. 69% of semiconductor respondents and 56% of suppliers believe they can capture a future market opportunity with 10%-30% power savings from SOI.

More than half (56%) of all respondents are unsure if their available EDA tools support their SOI needs, hence, another clear opportunity for education regarding the availability of EDA tools for SOI. Thirty-two percent say that the tools they use do support SOI (Figure 30), but of the 32%, 19% haven't evaluated the

tools yet. This appears to be an area where EDA companies may find the need to communicate their tool availability to customers. More than half (54%) of semiconductor and 64% of supplier respondents are not sure if their EDA tools support SOI. But 34% of semiconductor respondents indicate the EDA tools they have can support SOI, but of that, 19% have not evaluated them to confirm this belief. On the supplier side, 30% believe they support SOI, but 24% have not evaluated them.

**Are EDA tools available for your needs today?**  
(n=106)

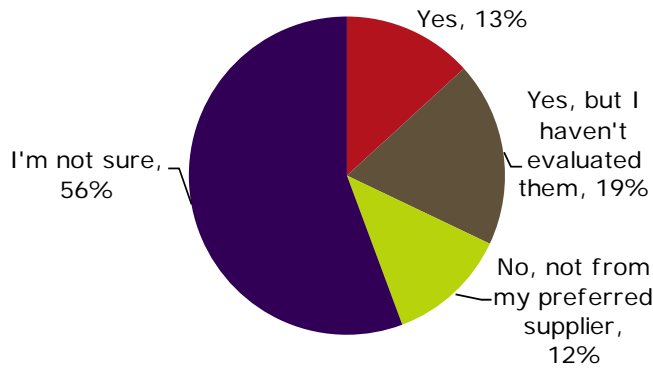
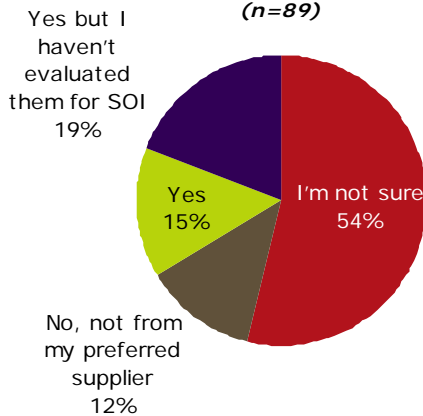


Figure 30. A majority responded that they are not sure if EDA tools support SOI (56%). But 32% of all respondents indicate the EDA tools they have can support SOI, but of the 32%, 19% have not evaluated them to confirm this belief.

**SEMICONDUCTOR**

**Are your EDA tools of choice available today to support SOI?**

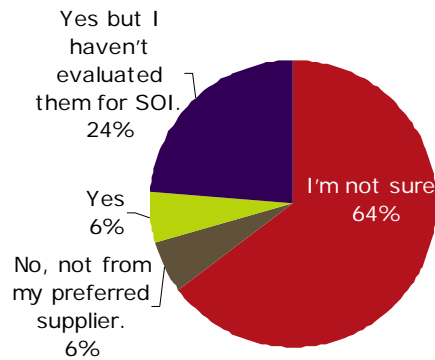
(n=89)



**SUPPLIER SERVICES**

**Are your EDA tools of choice available today to support SOI?**

(n=17)



Figures 31-32. 54% of semiconductor and 64% of supplier respondents are not sure if their EDA tools support SOI. But 34% of semiconductor respondents indicate the EDA tools they have can support SOI, but

of that, 19% have not evaluated them to confirm this belief. On the supplier side, 30% believe they support SOI, but 24% have not evaluated them.

This survey concludes that a large majority view silicon-validated IP as important or very important before using the IP in an SOI project, and almost all areas of the ecosystem require further development to support the needs of the respondents (Figures 33 and 36). The strong interest in SOI shown from these users should signal to the ecosystem a need to understand more clearly their customers' interest in specific tools, IP, foundry and technology node choices. In particular, there is a need for more SOI libraries at different technology nodes and for greater choice of silicon suppliers (Figure 36). Survey results for semiconductor (47%) and supplier (24%) respondents indicate a need for more SOI libraries for the silicon supplier they use and at the technology node they need (Figures 37 and 38).

**ALL RESPONSES**  
**What is missing in your design flow for SOI?**  
*(n=94)*

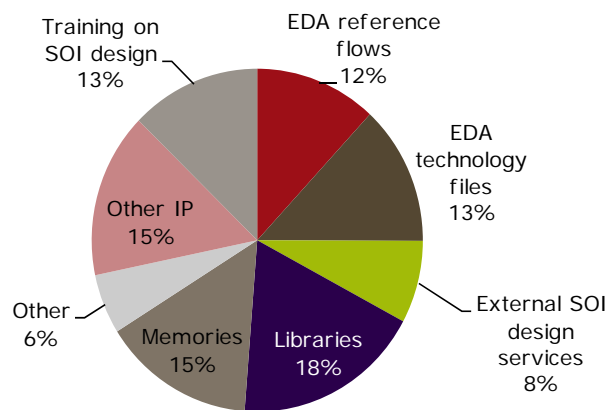
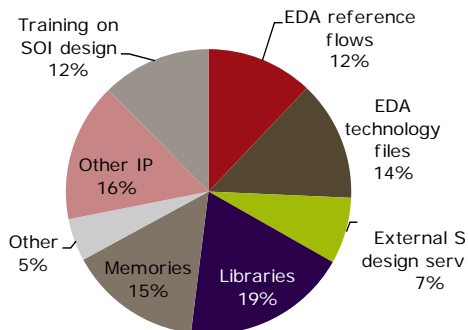
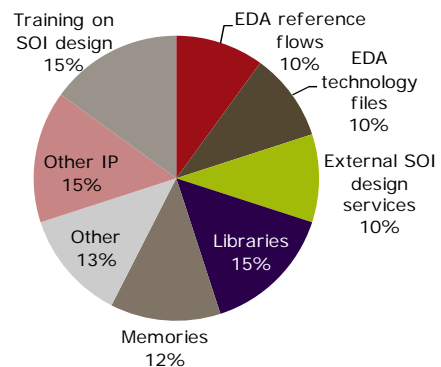


Figure 33. IP libraries lead the list of missing pieces in respondents' SOI design flow today.

**SEMICONDUCTOR**  
**What is missing in your design flow for SOI?**  
*(n=80)*



**SUPPLIER SERVICES**  
**What is missing in your design flow for SOI?**  
*(n=14)*



Figures 34-35. IP libraries continue to lead the list of missing pieces in semiconductor and supplier respondents' SOI design flow today at 19% and 15%, respectively.

**Are SOI libraries available for your needs today?**  
(n=97)

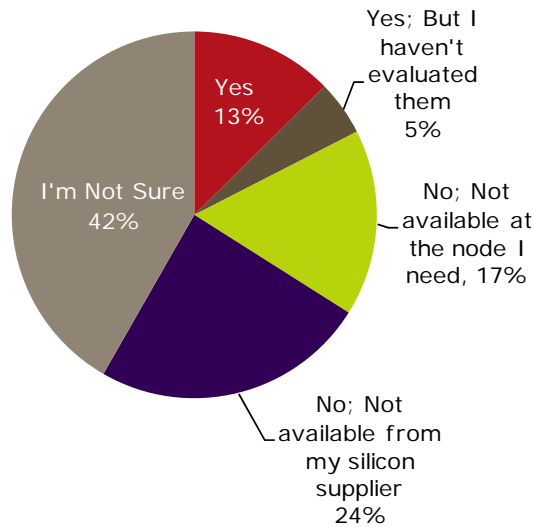
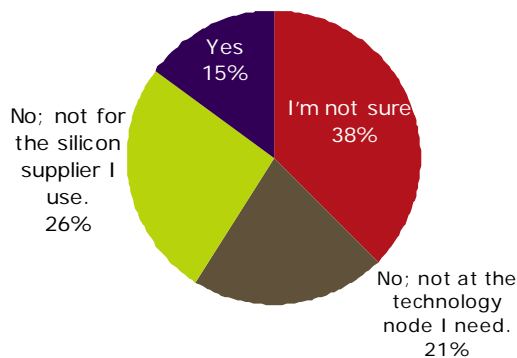
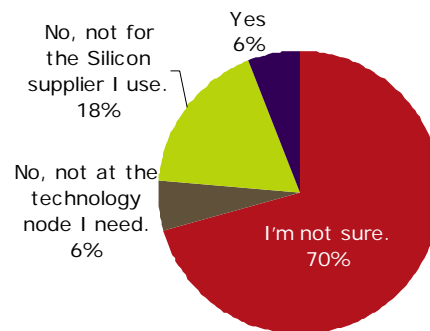


Figure 36. Survey results indicate a need for more SOI libraries for a greater choice of silicon suppliers and technology nodes.

**SEMICONDUCTOR**  
Are SOI libraries available for your evaluation today?  
(n=80)



**SUPPLIER SERVICES**  
Are SOI libraries available for your evaluation today?  
(n=17)



Figures 37-38. Survey results for semiconductor (47%) and supplier (24%) respondents indicate a need for more SOI libraries for the silicon supplier they use and at the technology node they need.

**Survey Counters Perception that SOI Interest is Only Leading Edge**

As is often the case, new technology tends to be evaluated by the leading-edge design teams with the budget and staffing to invest in such activity, and with market opportunities large enough to substantiate the

cost. This has been the perception for SOI adoption as well, that the next generation would be the transition point. However, the response to this survey indicates a large opportunity at process nodes in production today. Nearly three-quarters (74%) of the respondents represent small- to mid-size companies (Figure 39) using mainstream technology. As a result of their strong interest, 72% of the respondents indicated they would consider the transition to SOI at 90-nanometer, 65-nanometer or 45-nanometer technology today (Figure 42). Furthermore, 51% of respondents indicated that they would consider one or more designs using SOI at 45-nanometer. Currently, 22% of respondents indicated that they are already designing at 45-nanometer, while 29% predict they plan to use 45-nanometer within two years (Figure 45).

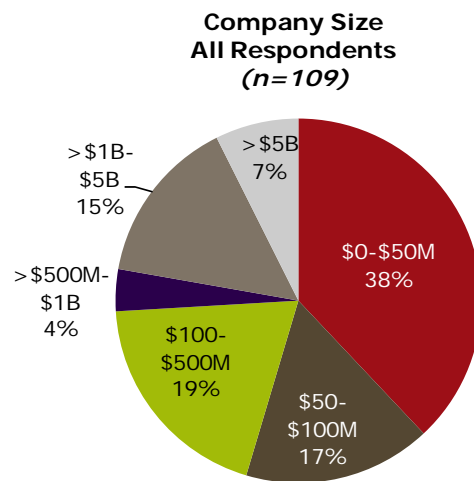
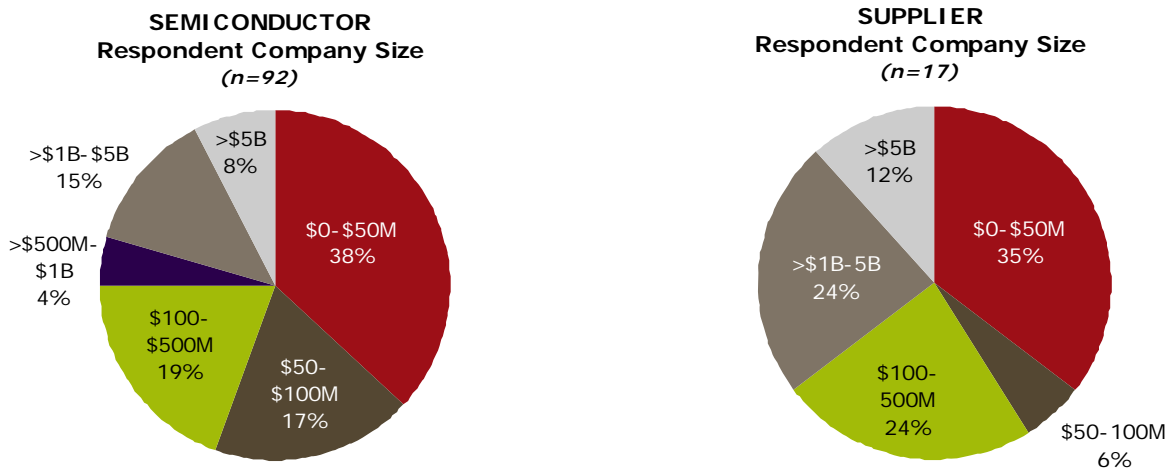


Figure 39. The majority of all respondents to this survey represent small-to-medium-sized companies. Nearly three-quarters of respondents represent companies with less than \$500M in annual revenues.



Figures 40-41. The majority of respondents to this survey for both semiconductor and supplier companies represent small-to-medium-sized companies with 74% of semiconductor and 65% of suppliers within this size range.

**ALL RESPONSES**  
**At which technology node would you consider a transition to SOI?**  
*(n=93)*

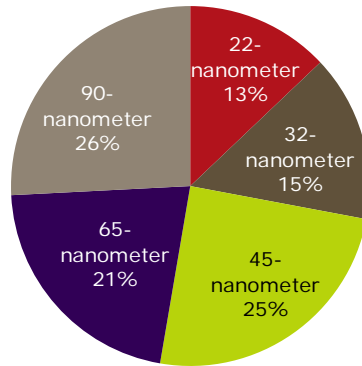
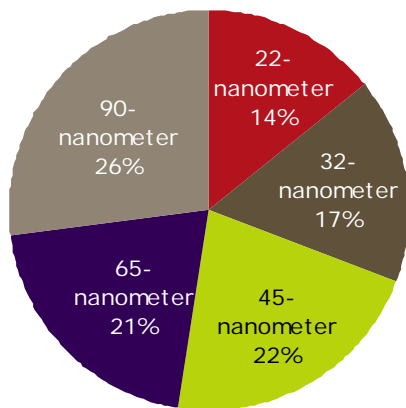
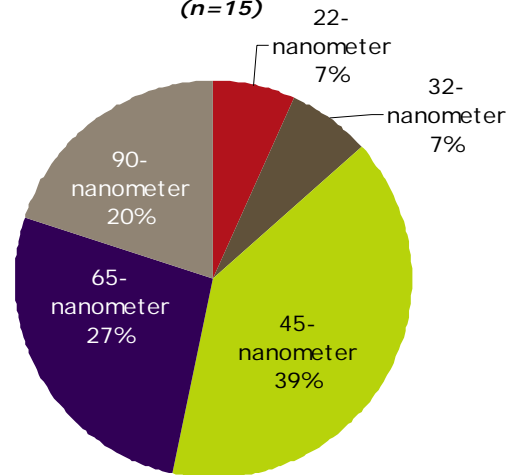


Figure 42. More than 70% of respondents identify mainstream technology nodes from 90-nm to 45-nm as possible transition points to SOI.

**SEMICONDUCTOR**  
**At which technology node would you consider a transition to SOI?**  
*(n=78)*



**SUPPLIER**  
**At which technology node would you consider a transition to SOI?**  
*(n=15)*



Figures 43-44. 69% of semiconductor and 86% of supplier respondents identify mainstream technology nodes from 90-nm to 45-nm as possible transition points to SOI.

**ALL RESPONSES**  
**When will you start designing in 45-nm?**  
*(n=103)*

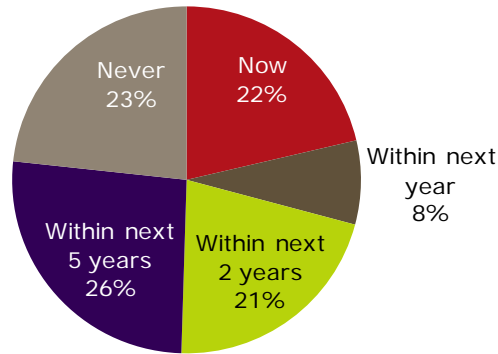
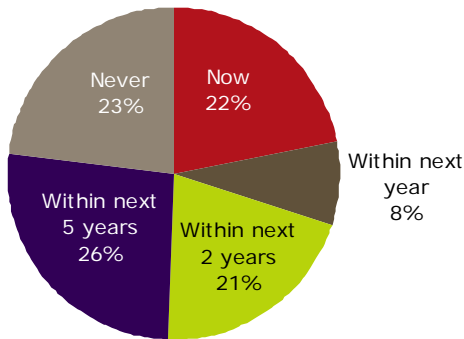
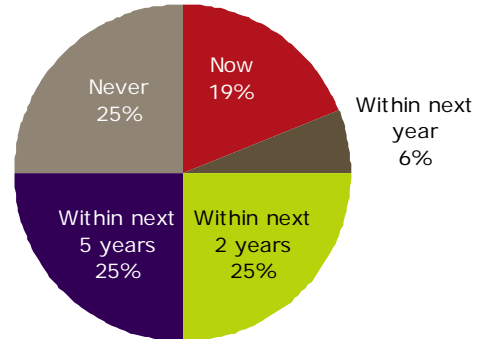


Figure 45. Today, 22% of respondents are using 45-nm and an additional 29% expect to use 45-nm within two years.

**SEMI CONDUCTOR**  
**When will you start designing in 45-nm?**  
*(n=87)*



**SUPPLIER**  
**When will you start designing in 45-nm?**  
*(n=16)*



Figures 46-47. Today, 22% of semiconductor respondents are using 45-nm, and an additional 29% expect to use 45-nm within two years. Only 19% of suppliers are at 45-nm today, but 31% expect to use 45-nm within two years.

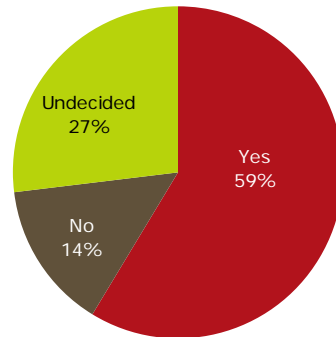
### Conclusion

In conclusion, this survey provides valuable insight into the perceptions, awareness and information gaps of a relevant group of designers not currently using but are interested in SOI. The survey respondents are interested in SOI because of potential power savings, followed by performance gains. They are also mainstream users today who are interested in evaluating SOI today, not tomorrow. These results reflect a need for the ecosystem to rally to support their customers' interest in SOI.

Education is key to reducing barriers to adoption, and the survey findings also confirm the need for a group dedicated to SOI to provide the knowledge and expertise needed to inform the industry and debunk present misconceptions.

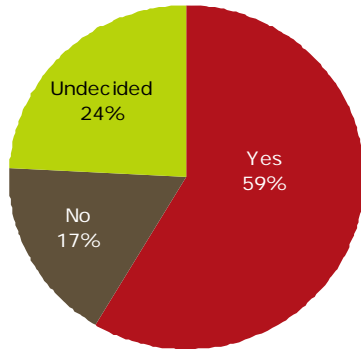
More than 60 respondents indicated they would like to attend a seminar on design and use of SOI (Figure 48). Further opportunities and priorities were indicated through responses to questions about helpful aids, reasons for not evaluating SOI and more specific questions about their understanding of IP and EDA tool availability.

**ALL RESPONSES**  
**Would a seminar on "Design and Use of SOI" be helpful for your decision?**  
*(n=104)*

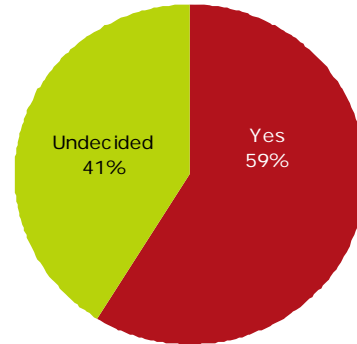


*Figure 48. More than 60% of respondents indicate a seminar on SOI design and use would be helpful.*

**SEMICONDUCTOR**  
 Would a seminar on "Design and Use of SOI" be helpful for your decision?  
 (n=87)



**SUPPLIER**  
 Would a seminar on "Design and Use of SOI" be helpful for your decision?  
 (n=17)



Figures 49-50. 59% of both semiconductor and supplier respondents indicate a seminar on SOI design and use would be helpful.

**METHODOLOGY**

GSA surveyed semiconductor suppliers, design services providers, systems companies, IP providers, EDA providers, silicon suppliers, equipment suppliers, back-end services suppliers around the world to gauge industry awareness and perception of SOI Technology. The survey garnered 110 valid industry respondents holding the following titles. Chief Executive Officer, Chief Technical Officer, Director of Engineering, VP of Engineering, VP of Operations, and other engineering contacts. Eighty-five percent of companies were responsible for the design of integrated circuits (ICs).

Semiconductor respondents included: Semiconductor suppliers, design services providers and systems companies. Supplier companies included. IP providers, EDA providers, silicon suppliers (wafer foundries), equipment suppliers, back-end services suppliers.

**WHAT IS SOI?**

According to the SOI Consortium, silicon-on-insulator (SOI) technology electrically insulates a fine layer of the monocrystalline silicon from the rest of the silicon wafer. This opens up new opportunities for innovation, delivering performance, power and area (PPA) advantages that bulk CMOS technologies cannot easily match. The SOI manufacturing process is actually simpler than bulk-based CMOS processes. In bulk, isolation and other processes continue to grow in complexity – and cost – with scaling. Recent studies indicate that overall SOI solutions can be cost-neutral – or even cheaper than bulk silicon.

**ABOUT GSA**

The Global Semiconductor Alliance (GSA) mission is to accelerate the growth and increase the return on invested capital of the global semiconductor industry by fostering a more effective fabless ecosystem through collaboration, integration and innovation. It addresses the challenges within the supply chain

including IP, EDA/design, wafer manufacturing, test and packaging to enable industry-wide solutions. Providing a platform for meaningful global collaboration, the Alliance identifies and articulates market opportunities, encourages and supports entrepreneurship, and provides members with comprehensive and unique market intelligence. Members include companies throughout the supply chain representing 25 countries across the globe. [www.gsaglobal.org](http://www.gsaglobal.org)

The survey was fielded and data collected by GSA. The segmented data and research analysis for this report was conducted in May 2008 by Lisa Tafoya, Vice President of Global Research for the Global Semiconductor Alliance (GSA). [Itafoya@gsaglobal.org](mailto:Itafoya@gsaglobal.org)

### **ABOUT THE SOI INDUSTRY CONSORTIUM**

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Representing leaders spanning the entire electronics industry infrastructure, SOI Industry Consortium charter members include: AMD, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, IBM, Innovative Silicon, KLA-Tencor, Lam Research, NXP, Samsung, Semico, Soitec, SEH Europe, STMicroelectronics, Synopsys, TSMC and UMC. Membership is open to all companies and institutions throughout the electronics industry. [www.soiconsortium.org](http://www.soiconsortium.org)

For more information about SOI Consortium, contact Camille Darnard-Dufour, Communications Contact. [camille.darnaud-dufour@soiconsortium.org](mailto:camille.darnaud-dufour@soiconsortium.org)

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