# Comparison study of FinFETs: SOI vs. Bulk

***Performance, Manufacturing Variability and Cost***

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# Goal of the Study

**To compare the performance, process variability, and cost of potential FinFET process flows based on SOI and bulk silicon wafers**

The study will show

- *Both SOI and bulk FinFETs should be able to achieve comparable performance.*
- *Bulk FinFETs will require a more complex doping implementation.*
- *Bulk FinFETs will have difficult variability control.*
- *The estimated cost differential of processed wafers using the Bulk and SOI substrates is within the accuracy of our projections.*

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# Discussion Outline

- **3 Cases (Proposed Flows):**
  - SOI FinFET
  - Bulk FinFET – Junction Isolation
  - Bulk FinFET – Material Isolation
- **Performance Analysis:**
  - Transistor performance
  - Parasitic element comparison
  - Leakage comparison
- **Variability Analysis**
- **Cost/Complexity Analysis**



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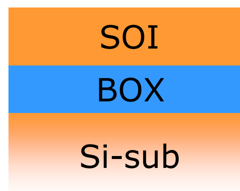
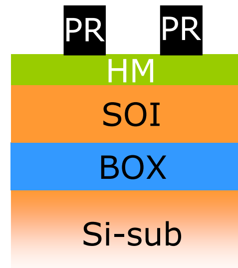
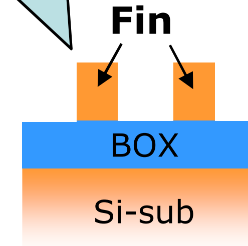
# Case 1:SOI FinFET flow

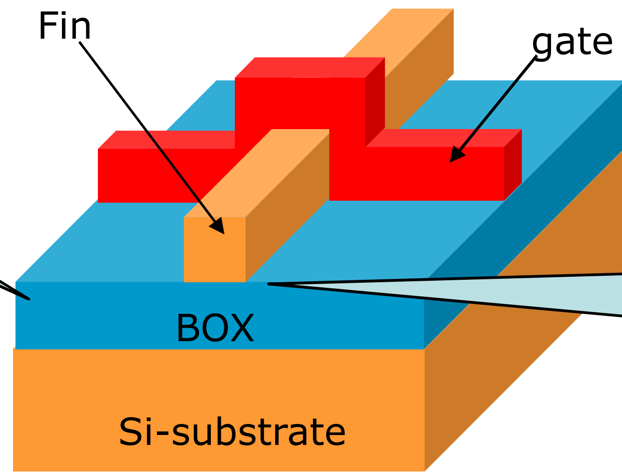
The fin trench etch simply stops on the wafer's buried oxide layer




Because of the buried oxide layer, adjacent fins are fully isolated from each other and no additional isolation steps are needed




In the fully-depleted, undoped-channel devices being considered for this node, only source and drain implants, followed by gate fabrication, are needed to complete the device

# Junction Isolated Bulk FinFET flow

Si-sub
HM
Si-sub
HM HM
Si-sub
oxide
HM HM
Si-sub
HM HM
Si-sub
Fin
Si-sub

The oxide deposition must fill a deep, high aspect ratio trench

Timed etch

Oxide provides insulation between adjacent fins, the transistors are still connected underneath the oxide. A high dose junction implant at the base of the fin completes the isolation

Fin
gate
oxide
Si-substrate

**Bulk-FinFET (“junction isolated”)**

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## Material Isolated Bulk FinFET flow

Si-sub

PR PR
HM
Si-sub

HM HM
Si-sub

oxide
HM HM
Si-sub

HM HM
Si-sub

HM HM
Si-sub

HM HM
Si-sub

HM HM
Si-sub

Si-sub
**Fin**

Fin
gate
oxide
Si-substrate

**Bulk-FinFET ("material isolated")**

- Oxide is allowed to grow from the oxide trench isolation across the bottom of the fin.
- Because of its complexity, we do not expect the material isolation approach will be viable for manufacturing and have not analyzed it as closely.

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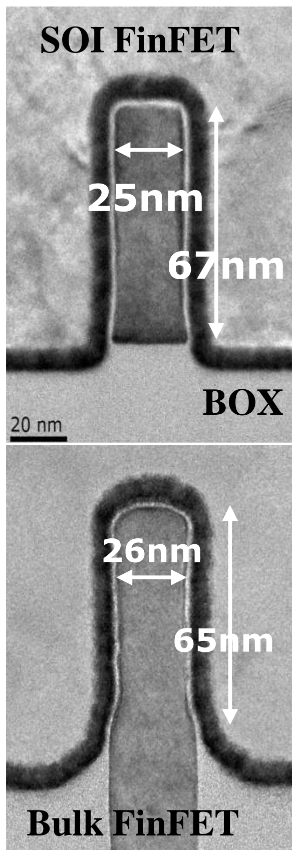
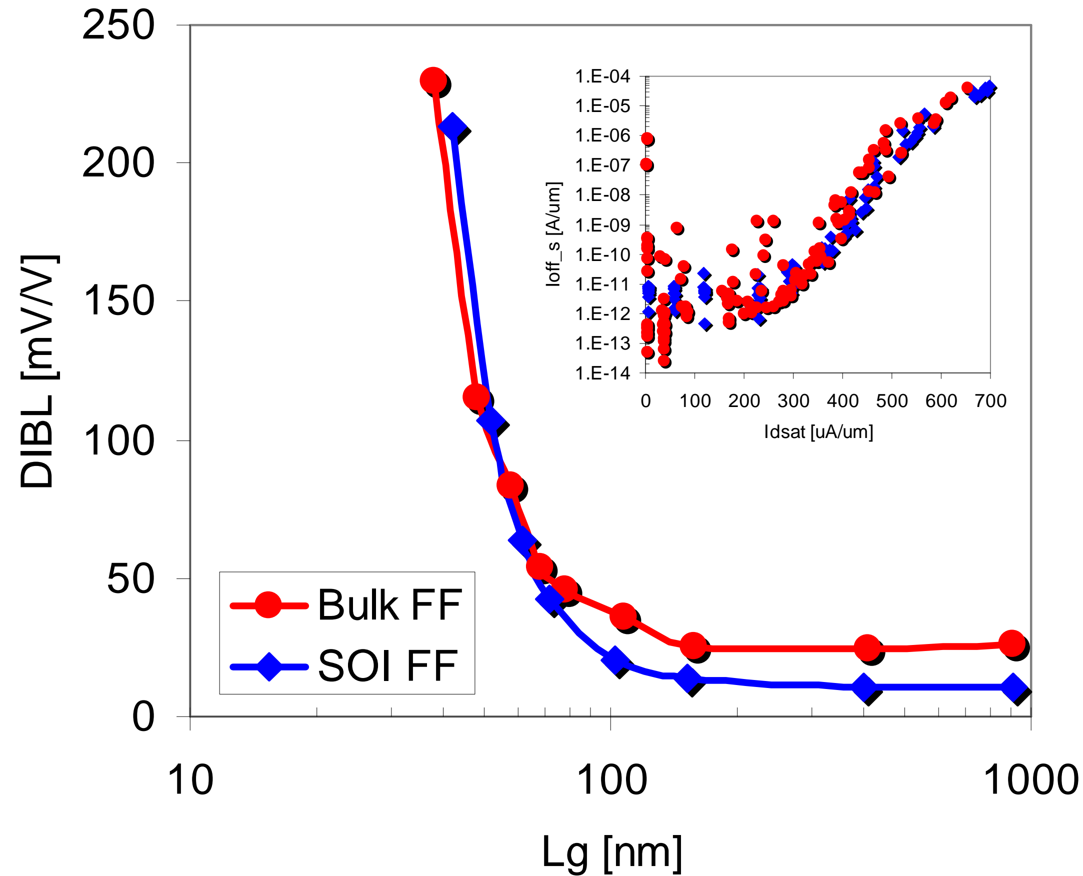
# DC performance benchmarking

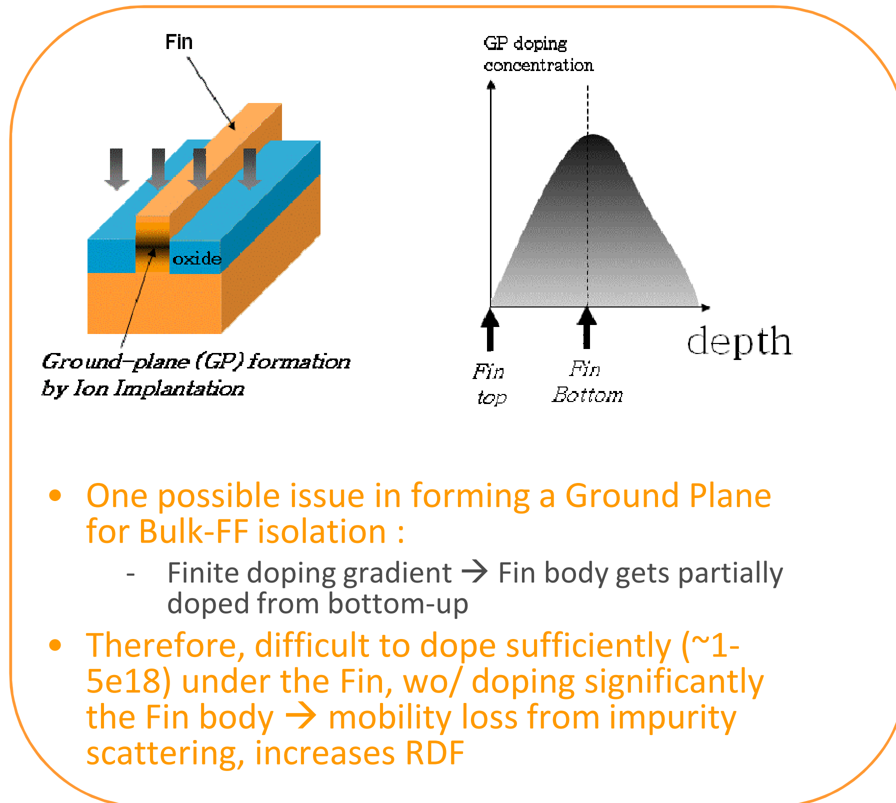


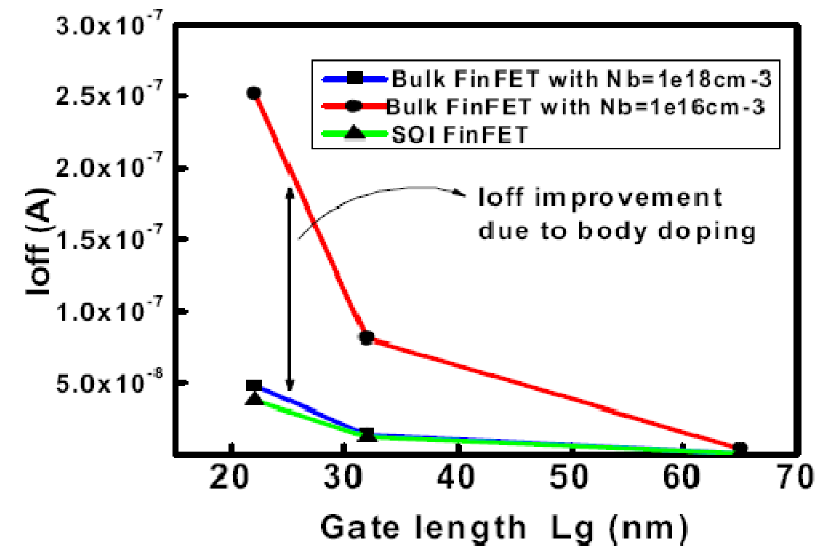

Parvais *et al.*, VLSI-TSA, 2009




At matched (Wfin, Hfin) → equivalent performance & SCE for SOI-FF and Bulk-FF

# Leakage comparison




Manoj *et al*., IEEE TED. 2008

- **Junction isolated Bulk-FF can potentially match SOI in terms of sub-VT leakage control, but doping optimization can be complex**

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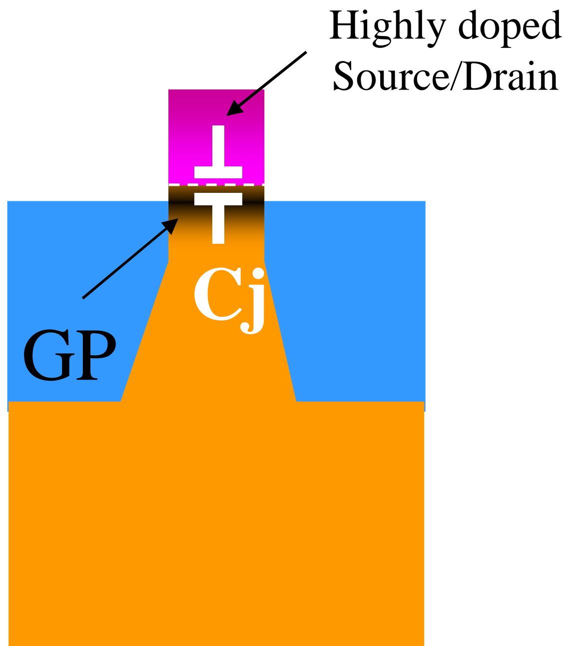
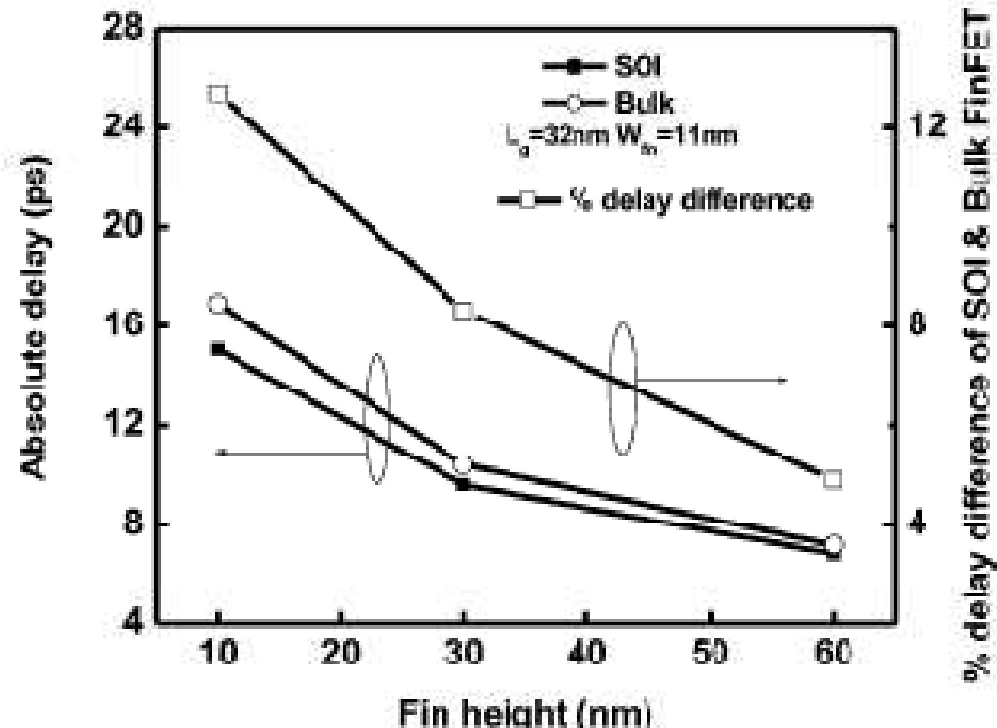
# Parasitics capacitance & AC performance

Manoj *et al.*, IEEE TED. 2008




- **Junction isolated Bulk-FF has intrinsically more parasitic capacitance than SOI (due to junction capacitance)**
  - **Cf. work from Manoj et al., IEEE TED'08**
- **However, if Hfin > 40-50nm, the impact of the junction capacitance penalty of Bulk-FF over SOI-FF (in terms of RO delay) can be kept below ~5-6%**



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- Cost/Complexity Analysis



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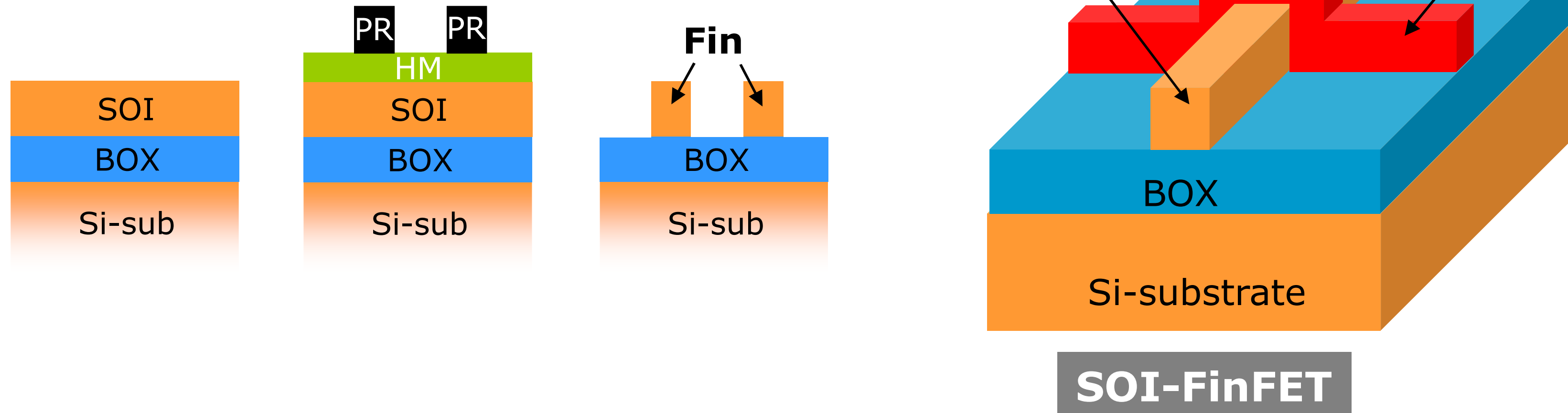
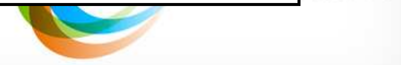
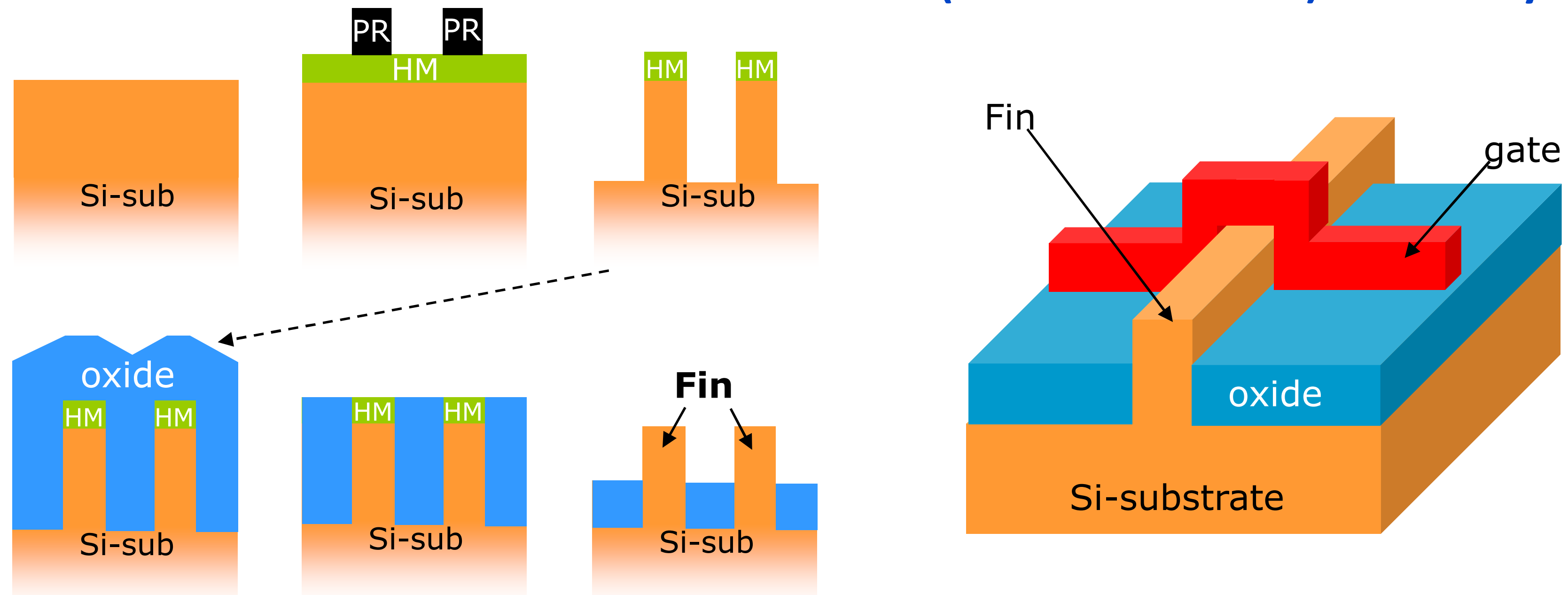
# SOI FinFET Variability




| Sources of Variability | Unit | Nominal | 3-sigma Tolerance (current) | 3-sigma Tolerance (future) | |
|---|---|---|---|---|---|
| SOI Layer | nm | 70 | 2 | 1 | 5% 3sigma SOI thickness variability with future improvements in high volume manufacturing |
| Hardmask dep | nm | 10 | 1 | 0.5 | 10% cross-wafer 3sigma |
| Fin Etch | nm | 70 | 4.2 | 2.1 | 5% cross wafer + 1% overetch |
| Corner rounding | nm | 2 | 0.1 | 0.05 | |
| **Total fin height variability (nm)** | | | **4.8** | **2.4** | Root sum-square of all sources of variability |
| **Total fin width variability (nm)** | | | **1.0** | **0.5** | In 32nm technology, active area CD variability is 15nm across iso-dense patterns, multiple pitchs and RIE overetch from variability in vertical layers. For FinFETs, most of the CD variability is expected to come from the overetch to account for thickness variability in Fin definition since the pitch will be fixed. Assumption is that 20% of the vertical variability will translate to CD (Fin width) variabiliy. |



# Bulk FinFET (Junction isolated) Variability




| Sources of Variability | Unit | Nominal | 3-sigma Tolerance (current) | 3-sigma Tolerance (future) | |
|---|---|---|---|---|---|
| HM oxide | nm | 8 | 0.4 | 0.2 | 5% 3sigma variation for oxide |
| HM nitride | nm | 70 | 7 | 3.5 | 10% 3sigma variation for deposited nitride |
| Trench etch | nm | 170 | 8.5 | 4.25 | 5% 3sigma from trench etch based on 32nm data |
| Oxide recess | nm | 100 | 5 | 2.5 | Oxide dry/wet etch with no etch stop. 100nm oxide etchback for 70nm fin height assumed. |
| Pad oxide | nm | 2 | 0.1 | 0.05 | |
| Well anneal | nm | 0 | 3 | 1.5 | 3sigma variability in junction depth from angled implants |
| **Total fin height variability (nm)** | | | **12.5** | **6.2** | Root sum-square of all sources of variability |
| **Total fin width variability (nm)** | | | **2.5** | **1.2** | Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability. See previous slide for more details on fin width variability. |

## Variability Comparison of SOI FinFETs vs Bulk FinFETs

| | SOI-based FinFET | | Junction-isolated bulk FinFET | |
|---|---|---|---|---|
| | Litho steps | Process steps | Litho steps | Process steps |
| FEOL process | 7 | 56 | 9 | 91 |

| | | SOI FF (nm) | Bulk-junction isolation FF (nm) | % variability relative to SOI |
|---|---|---|---|---|
| 3-sigma variability in Fin Height | current | 4.8 | 12.5 | 160 |
| | future | 2.4 | 6.2 | 158 |
| 3-sigma variability in Fin width | current | 1 | 2.5 | 150 |
| | future | 0.5 | 1.2 | 140 |

- **Fin height and fin width variability in bulk FinFETs (both material isolated and junction isolated versions) is expected to be ~140-170% higher compared to SOI FinFETs**

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- 3 Cases (Proposed Flows):
  - SOI FinFET
  - Bulk FinFET – Junction Isolation
  - Bulk FinFET – Material Isolation
- Performance Analysis:
  - Parasitic element comparison
  - Leakage comparison (Junction Isolation)
- Variability Analysis:
  - Effective Width Variation
- Cost/Complexity Analysis

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# Cost Analysis for FinFET on SOI vs. Bulk

| | FinFET on SOI | | | FinFET on Bulk | | | |
|---|---|---|---|---|---|---|---|
| | Litho Steps | Process steps | Cost | Litho Steps | Process steps | Cost | Delta Cost |
| Substrate | | | $500 | | | $120 | $380 |
| FEOL Process | 7 | 56 | $561 | 9 | 91 | $805 | -$244 |
| Total Cost difference | | | | | | | $136 |

Assumption:

1. All circuitries can be converted to the undoped channel FinFET architecture for both SOI and Bulk.
2. SOI substrate cost of $500 will be available in 2012 with high volume manufacturing
3. Generic FEOL process flows for FinFET on SOI and Bulk . Cost only included 1 gate dielectric thickness, 1 Vt for N- and PMOS to metal 1. No capacitors, resistors, eDRAM, ESD, I/O,…. Additional processes for fabrication of multi Vt, Dual or triple gate dielectric thickness, more circuitries and metal interconnect layers will add more process costs for both approaches.

# Bulk vs SOI FinFET Cost Analysis

% Cost Difference (Bulk-SOI)

Total Wafer Cost ($)

| Total Wafer Cost ($) | % Process cost (Bulk-SOI) | % Substrate cost (Bulk-SOI) | % Process+substrate cost (Bulk-SOI) |
|---|---|---|---|
| 4000 | 6.1% | -9.5% | -3.4% |
| 5000 | 4.9% | -7.6% | -2.7% |
| 6000 | 4.1% | -6.3% | -2.3% |
| 7000 | 3.5% | -5.4% | -1.9% |
| 8000 | 3.1% | -4.8% | -1.7% |

- The SOI finFET wafer cost increment over bulk depends on the final wafer cost.

# Summary

- **This** study **evaluated the performance, variability and cost differences between FinFETs fabricated with Bulk and SOI substrates. 3 process flows were compared:**
  - SOI FinFET
  - Bulk FinFET – Material Isolation
  - Bulk FinFET – Junction Isolation
- **Similar DC & AC performance for SOI-FF & Bulk-FF are observed**
  - Junction isolated Bulk-FF has intrinsically more parasitic capacitance than SOI but the impact of the junction capacitance penalty can be kept below ~5-6%
- **Doping appears more complex for Bulk-FF**
- **Fin height & Fin width variability appear to be significantly larger for Bulk-FinFET this lead important wafer manufacturing and product control challenges**
- **Our study indicates that at high-Volume the cost difference of SOI-FinFET over Bulk-FinFET is less than 4%**



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