



**SOI INDUSTRY CONSORTIUM ANNOUNCES SOI DESIGN CLINIC
AT ARM TECHCON3**

**New SOI Design Clinic To Be Held
on October 21, 2009 in Santa Clara, California**

BOSTON, MASS., October 8, 2009 – The [SOI Industry Consortium](#) today announced an initiative to deliver a silicon on insulator (SOI) educational event in conjunction with ARM TechCon³ to help the electronics industry reap the benefits of SOI. Responding to the industry's need for education in this area, the SOI Design Clinic will provide IC designers and engineering management with a technical understanding of significant differences between designing on SOI versus bulk silicon, and how to receive the power-saving, integration, reliability and performance advantages of SOI. Respected experts from the semiconductor industry will deliver training and share their insights at this practical and timely event, to help attendees evaluate and plan their move to SOI.

Shrinking semiconductor feature sizes demonstrate that CMOS on bulk silicon is rapidly reaching its technological limits for many applications. Process complexity, variability, short-channel effects, leakage, power density, and reliability are just a few reasons why technology leaders transition to SOI. Today available foundry processes, libraries, EDA tools and designer training are making SOI accessible to fabless semiconductor companies and OEMs, and enabling first-time SOI design teams to achieve improved power, performance and area results in their customary design cycle times, as documented by ARM in a recent study released today (<http://www.arm.com/news/26070.html> .)

The design clinic will take place in the Santa Clara Convention Center (California) on October 21, 2009, co-located with ARM TechCon³. Presented in two 3 hour sessions of live classroom instruction, from 9am to 12noon and from 2pm to 5pm, the program will include lunch, admission to the ARM TechCon³ keynote session and a post-clinic reception on the exhibition floor. The design clinic content will focus on:

- SOI fundamentals
- Current and emerging bulk CMOS design challenges and how SOI eliminates/mitigates them
- Lower power design techniques
- High performance microprocessor system design techniques
- PDKs, libraries, IP and EDA tool ecosystem for SOI design
- Standard cell/custom design flows and methodologies
- Projections for the future of SOI design

Readers can visit <http://soidesignclinic.com> to review program details and register for the event.

The SOI Industry Consortium welcomes companies, organizations, government and academic institutions to join the group in applying the full benefits of SOI-based electronics to global sustainability challenges and lowering the total cost-of-ownership of electronics. To find out more, to join or to arrange for a company-specific design clinic, please visit www.soiconsortium.org.

About the SOI Industry Consortium:

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Representing innovation leaders from the entire electronics industry infrastructure, current SOI Industry Consortium members include: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, GLOBALFOUNDRIES, IBM, IMEC, Infotech, Innovative Silicon, Kanazawa Institute of Technology, College of Engineering , KLA-Tencor, Magma Design, Nvidia, Ritsumeikan University, Samsung, Semico, SEH Europe, Soitec, Stanford University, STMicroelectronics, Synopsys, TSMC, Tyndall Institute, University of California-Berkeley, University Catholique de Louvain, UMC and Varian. Membership is open to all companies and institutions throughout the electronics industry. For more information, please visit www.soiconsortium.org.

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