

Design Methodology for FinFET GG-NMOS ESD Protection Devices

S. Thijs⁽¹⁾, C. Russ⁽²⁾, D. Trémouilles⁽³⁾, D. Linten, M. Scholz, M. Jurczak, N. Collaert,
R. Rooyackers, C. Duvvury⁽⁴⁾, H. Gossner⁽²⁾ and G. Groeseneken⁽¹⁾

Email: Steven.Thijs@imec.be, Tel: + 32 16 28 7749, Fax: +32 16 28 1706
IMEC vzw, Kapeldreef 75, Leuven, B-3001, Belgium

(1) also at: Electrical Engineering Dept., Katholieke Universiteit Leuven,
(2) Infineon Technologies, (3) LAAS/CNRS, (4) Texas Instruments Inc.

Abstract –In this paper, a design methodology is presented which takes into account all complex dependencies of the electrical ESD device parameters of a Grounded-Gate-NMOS FinFET device on its layout parameters. This allows finding the minimum area solution which fulfills all imposed design constraints.

I. Introduction

The FinFET transistor is the most widely studied multi-gate architecture for technology-scaling below 45 nm due to its excellent control of Short Channel Effects (SCE) and its compatibility with standard CMOS processing. In [1], the different ESD device parameters (failure current I_{t2} , holding voltage V_h , on-resistance R_{on} , leakage current and area consumption) of a Grounded-Gate-NMOS FinFET device were investigated as a function of different layout and process parameters. While process options are generally imposed by the technology, the ESD design engineer can only change the layout parameters to find an optimal ESD layout and design strategy.

II. Design Methodology

In Figure 1, a top view is shown of a FinFET device, together with the different layout parameters. The fin width W_{fin} , gate length L_G , contact area L_{cont} and number of fins N can be chosen by the designer. Distance between landing pad and gate L_{SD} , overlap gate on fins W_{ext} and fin-to-fin spacing S are fixed by the process.

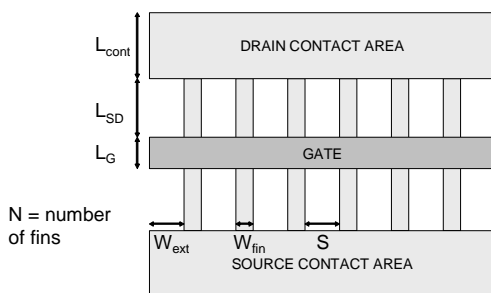


Figure 1: Top layout view of a FinFET device

The impact of W_{fin} and L_G on the different ESD device parameters as presented in [1] are summarized in Table 1. A “+” indicates behavior beneficial for ESD, whereas a “-” indicates a detrimental effect. Two different normalizations are used for I_{t2} as in [1]. The effective silicon width does not include the fin-to-fin

spacing (parameter S in Figure 1), whereas the total layout width does.

Table 1. Summary of different device parameters as a function of layout parameters gate length and fin width. “+” indicates beneficial for ESD, whereas “-” indicates a detrimental effect.

	Short Lg	Long Lg
Narrow fin	+ Low V_h + Low R_{on} + Low leakage - Low $I_{t2}/\text{layout width}$ + High $I_{t2}/\text{eff. width}$	Medium V_h Medium R_{on} + Low leakage Medium $I_{t2}/\text{layout width}$ + High $I_{t2}/\text{eff. width}$
Wide fin	+ Low V_h Medium R_{on} - High leakage Medium $I_{t2}/\text{layout width}$ Medium $I_{t2}/\text{eff. width}$	- High V_h - High R_{on} + Low leakage Medium $I_{t2}/\text{layout width}$ Medium $I_{t2}/\text{eff. width}$

Ultimately, the goal is to find the minimum area solution of a MOS clamp in bipolar mode which can sustain a certain ESD stress, while meeting a given leakage specification and without exceeding a certain maximum voltage V_{max} during ESD.

Based on available measurement data for devices with certain W_{fin} and L_G , I_{t2} , V_h and R_{on} are calculated over the full L_G - W_{fin} -design space using a Delaunay interpolation method.

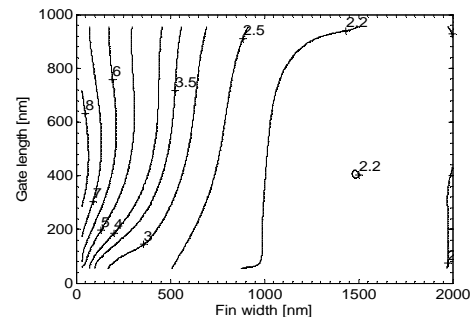


Figure 2: Contour plot of normalized failure current I_{t2} per effective silicon width [mA/μm] as a function of L_G and W_{fin} .

Figure 2 shows a contour plot of I_{t2} , normalized per effective silicon width, over the L_G - W_{fin} design space. At large W_{fin} , I_{t2} saturates around 2 mA/μm. Contour

plots of V_h and R_{on} are shown in Figure 3 and Figure 4 respectively according to [1].

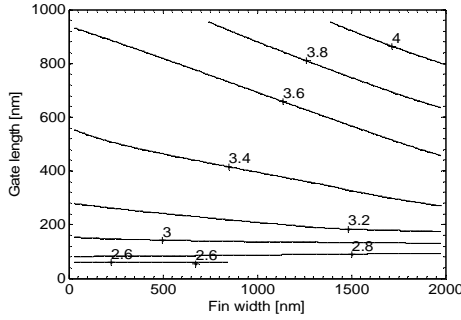


Figure 3: Holding voltage V_h [V] contours as a function of L_G and W_{fin}

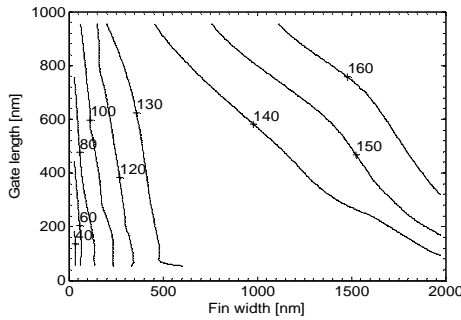


Figure 4: Normalized on-resistance R_{on} contours per effective silicon width [$\Omega\mu m$] as a function of L_G and W_{fin}

Leakage qualification is done based on an empirical formula (1), where Short Channel Control (SCC) is calculated as a function of L_G , W_{fin} and equivalent oxide thickness (EOT). $SCC > 1.4$ is considered as a safe device, $SCC > 1$ has still good short channel control, while devices with $SCC < 1$ suffer from strong SCE.

$$SCC = \frac{L_g}{[\min(W_{fin}, 2H_{fin}) + 6EOT]} \quad (1)$$

$$V_{drop} = V_h + I_{ESD} R_{tot} < V_{max} \quad (2)$$

The voltage drop over the device during maximum ESD current is calculated using (2) where R_{tot} represents the total resistance of the device. V_{drop} has to remain below the maximum allowed voltage in the application V_{max} and the number of fins N can be increased to reduce R_{tot} when necessary. The total necessary device area is calculated as in (3).

$$Area = (NW_{fin} + (N-1)S + 2W_{ext})(L_g + 2L_{SD} + 2L_{cont}) \quad (3)$$

III. Design Application

As an example, the design methodology described in the previous section can be used to determine the minimum area solution for a GGNMOS device with an ESD capability of 1 kV HBM, V_{max} of 4 V during ESD and low leakage current (excellent SCC). The required area is calculated using (3) for each point in the L_G - W_{fin} design space. The optimal solution is the point in the L_G - W_{fin} design space with the smallest required area. Figure 5 shows the percentage of area increase over the optimal solution, which is indicated by the dot. The

optimal solution has 395 nm L_G and 200 nm W_{fin} . It is clear that any L_G or W_{fin} deviation from the optimum leads to a drastic increase in required area. No solutions exist for small L_G because of the leakage limitation and for large L_G because of too high voltages. The consumed area is $296 \mu m^2$.

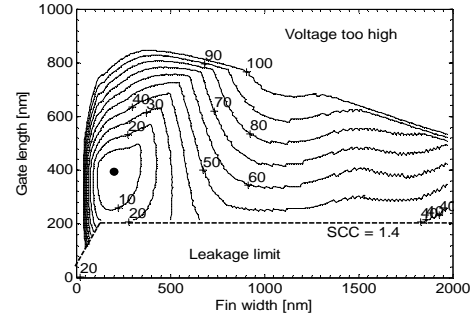


Figure 5: Percentage increased area over optimal solution (dot) which meets imposed design constraints of 1 kV HBM, 4 V V_{max} and excellent short-channel control ($SCC > 1.4$)

When the allowed voltage is decreased from 4 V to 3.4 V, the optimum solution shifts to lower L_G (165 nm) because of a lower required V_h . As a consequence, also W_{fin} (100 nm) has to be reduced for SCC, as seen in Figure 6. This results in an increased area consumption: $417 \mu m^2$.

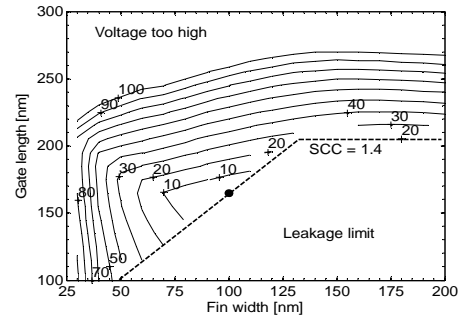


Figure 6: Percentage increased area over optimal solution (dot) which meets imposed design constraints of 1 kV HBM, 3.4 V V_{max} and excellent short-channel control ($SCC > 1.4$)

IV. Conclusions

This work demonstrated a design methodology to take into account all complex dependencies of the ESD device parameters of a Grounded-Gate-NMOS FinFET device on its layout parameters W_{fin} and L_G . This method allows finding a minimum area solution which meets given design constraints. Because technology keeps on changing, the different dependencies will change as well. However, the presented design methodology will remain valid as long as there is one or multiple trade-offs to be considered. A similar methodology can also be used for optimal active clamp or output driver design.

V. References

- [1] Trémouilles et al., "Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications", ESD 2007, pp408-415