

SOI implementation guide

methodologies for comparing bulk and SOI process technologies for SoC designs

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Silicon-on-insulator (SOI) process technologies have been used to implement high-performance, cutting-edge, custom designs, such as microprocessors, for several process generations. The benefits of SOI demonstrated by these designs – higher performance with the same power consumption, or lower power consumption with the same performance – have made SOI an attractive alternative for more mainstream designs as well.

Many SOC design teams using standard tool flows are starting to look to SOI. However, these teams often have questions about how to evaluate the potential gains they might realize by moving to an SOI process. Is a simulation-based comparison adequate, or is test silicon the only accurate method? What is the best way to set up a simulation-based comparison? What kinds of test circuits will give them the best idea of how SOI might impact their own design? What libraries should they use for these comparisons?

This paper will attempt to answer these questions and provide a methodology for comparison between bulk and SOI processes for design teams investigating the possible benefits of SOI for their designs.

making a fair but real-world comparison

Whenever an engineering team sets up a comparison between process technologies, it has two primary – and sometimes competing – concerns: to create the most “equal” comparison possible (apples to apples), and to conduct the comparison in a way that addresses actual design style and goals.

Comparisons between bulk and SOI processes highlight the tension between these two concerns. For example, if a comparison is not made on a level playing field, the results are suspect. On the other hand, the inherent differences between bulk and SOI processes are the source of potential performance or power improvements, so totally eliminating the effects of these differences negates the motivation behind the comparison.

Both bulk and SOI processes have their relative strengths and weaknesses. In the real world, design teams will always want to optimize their designs to take advantage of those strengths and to minimize the impact of those weaknesses. The key to a useful comparison is to optimize each process as much as possible, and compare those optimized results.

In order to isolate the benefits of the process from any other optimization, however, some “equalization” is necessary. Both processes should have matched:

- Technology generation (e.g.: 45nm)
- Design rule optimization for the technology generation (i.e.: are the design rules optimized to support area vs. performance scaling?)
- targeted transistor type (ie: low power vs. high performance, which relates back to relative process complexity and cost)
- poly gate length
- sub-threshold and gate dielectric leakages

With these factors consistent between both processes, and the design approach to each process optimized for its inherent strengths, design teams should be able to get a fair, but real-world comparison.

what to compare

The next question is 'what to compare?'. There are performance, power, and area trade-offs which would be of interest to design teams. A purely dc comparison of transistor characteristics is not representative of real circuit-level performance. SOI provides lower junction capacitances, the effect of which can only be seen in ac comparisons. Likewise, self-heating reduces the value of dc drive currents in SOI but is not relevant in most circuit applications. Also, SOI eliminates the back-bias effect, the impact of which is seen primarily in stacked gates, so this much should be captured in the comparisons.

CV/I performance benchmark comparisons are an improvement, but it is difficult to capture all the SOI capacitance and floating body advantages in such a simple metric. Performance comparisons of small gates have significant value, though it needs to be emphasized that not all these differences directly translate to product-level improvements. RLM blocks and speed paths from actual circuit examples are probably most relevant for understanding the impact of SOI at product-level. For RLM's, 10K-gates would be the smallest desirable, but there is a rule of thumb of 1% of full-chip gate count in looking for reasonable comparisons. Since the focus is on SOC designs, the RLM blocks and speed paths should be constructed out of representative standard cells.

A hierarchy of ac comparisons can be described: chains or rings constructed of a single gate type (inverter, NAND, NOR...), chains or rings using an assortment of different gate types selected to represent realistic circuit paths, random logic macro's (RLM's) chosen from an actual SOC implementation and critical speed paths chosen from actual STA timing runs. Clearly the further one moves up the hierarchy, the more representative the results will be of actual circuit impact, but the more effort it will require. Complex circuits that represent the design style of the ultimate product are the best comparison vehicles. Usually, a critical path from the design under consideration is the best test of how either bulk or SOI will perform for that design.

In running simulation comparisons of simple gates or more complicated speed-paths, it is important to include parasitics extracted from actual layouts, to better comprehend the differences in junction capacitance between SOI and bulk. Circuit simulator models for SOI have been optimized to include floating-body and history effects, thermal heating, and improved impact ionization models to better model the kink-effect. It is probably necessary to use actual bulk and SOI models for any simulation comparisons.

At a higher level of sophistication, the RLM's or speed paths could actually be run through a standard logic design flow, with synthesis, place-and-route, and timing. One of the difficulties of this is ensuring that the standard cells are extracted and timed using the appropriate SOI vs. bulk decks and models and using exactly the same assumptions (typical vs. worst case, level of additional loading...). If this can be assured, then valuable information about performance and area can be obtained.

Silicon-based comparisons are clearly better than simulation, but are often difficult to carry out. Multiple teams have seen simulation and silicon compare to within 5% with careful model and parasitic extraction.

If bulk and SOI processes exist at the same technology node and if the design rules, design kits, models are all consistent; the design team can perform the comparisons on a selected circuit block. This approach is highly recommended.

It should be noted that while the potential area savings with SOI vs. bulk in a logic block can be extracted from some of the above comparisons, chip-level area impact also requires that memories, analog blocks, and I/O's be taken-into account, which is beyond the scope of this article.

library design selection

A second question revolves around the circuits that should be used for comparisons – std. cells or custom design blocks. While much of SOI design was historically focused on custom microprocessor circuit blocks, a std. cell-based design is more relevant to SOC-design teams. For a common technology generation, design rule optimization, and std. cell design point (high-density vs. high-performance), a cell template can be communize (track height, cell height in tracks, etc.). SOI transistors don't require a well tie, which provides some area advantage. In most modern bulk std. cell libraries, however, well ties are separate cells and are not required very often for latch-up prevention so the area impact is not large. Historically SOI also allows some reduction of n+ to p+ spacing, which also results in area savings. It should be noted that salicided poly interdiffusion limits scaling in the y-direction (perpendicular to current flow) and starting at 65nm for high-performance technologies and 32nm for low-power, poly and active pitches are becoming restricted in order to further improve patterning (ACLV). The simplest approach then is to use exactly the same std. cell library.

examples of SOI vs. bulk comparisons

ARM, working with UMC provided an example of a library based comparison at 65nm. Using a common set of design rules, ARM laid-out a subset of cells for both a 9- and 12-track library. Chains were constructed of a variety of gates (nand2, nor2, mux, inverter) for both track heights and for cell strengths from 1x to 8x. A constant wire-load was used for all cell strengths. Parasitics were extracted from layout and SPICE simulations carried out. The chains were also run on silicon and the agreement with simulation was within 5%. ARM saw a 15-29% frequency improvement for SOI over bulk at the same cell strength level. If frequency were held constant, they were able to achieve a 25% area reduction by trading off with smaller strength cells. This also led to a reduction in dynamic power of around 27%. Reducing the power supply voltage, followed by a smaller reduction in cell strength gave a somewhat larger dynamic power reduction (29%). In future generations, this option could be limited because of SRAM bitcell Vmin restrictions. Static power comparisons were challenging in this study since linear threshold was matched, but due to floating-body effects, saturated threshold was lower and off-leakage higher for SOI. It is possible with more careful transistor design to set the saturated thresholds of off-leakages the same between SOI and bulk.

summary and conclusions

This article describes a simple methodology for an SOC design team to carry-out a comparison study to understand the potential advantages of SOI over bulk. It is important that the SOI and bulk technologies be of the same technology generation and use the same type transistor (high-performance or low-power). AC performance comparisons are essential. These can be based just on simple gates, but this may somewhat overstate the impact on overall product performance, so representative RLM's and speed-paths are preferred. Silicon-based comparisons give more accurate results but are often impractical. Multiple teams have shown that simulations can be within 5% of silicon if a careful methodology is applied.