



THE SOI INDUSTRY CONSORTIUM LAUNCHES SOI IMPLEMENTATION GUIDE

BOSTON, MASS., September 16, 2008 – The SOI Industry Consortium, focused on accelerating silicon-on-insulator (SOI) innovation into broad markets, announced today the availability of the first chapters of its **SOI Implementation Guide**. The SOI Implementation Guide features a series of white papers and presentations from industry experts on specific topics to promote a common understanding of the value and challenges of SOI.

“Education is key to reducing barriers to adoption. Having easily accessible information is essential to providing the knowledge and expertise needed to inform the industry and eliminating present misconceptions,” said Horacio Mendez, executive director of the SOI Industry Consortium. “The ongoing creation of chapters for the SOI Implementation Guide represents great teamwork and individual contributions from the companies and academic and R&D organizations within our consortium.”

SOI process technologies have been used to implement high-performance, cutting-edge, custom designs, such as microprocessors, for several process generations. The benefits of SOI demonstrated by these designs – higher performance with the same power consumption, or lower power consumption with the same performance – have made SOI an attractive alternative for more mainstream designs as well.

The SOI Implementation Guide features subjects such as a methodology for comparing bulk and SOI process technologies for design teams investigating the potential benefits of SOI. Another chapter addresses the partially depleted SOI circuit design advantages such as improved chip performance and lower power consumption, as well as the design issues raised by the bulk CMOS circuit design community. Other upcoming chapters will cover subjects such as an SOI overview and assessment for Analog and Mixed Signal (including 6 individual chapters on the application of SOI to RF and Analog), SOI cost analysis, FinFets and SOI, SRAM scalability in bulk and SOI, followed by a guide on how to port IP from bulk to SOI.

The SOI Industry Consortium is open to any company, organization or academic institution with an interest in SOI. Certain chapters of the Implementation Guide will initially be available to members only; the rest will be available to the general public on the consortium’s website:

www.soiconsortium.org

About the SOI Industry Consortium:

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Representing leaders spanning the entire electronics industry infrastructure, SOI Industry Consortium members include: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Chartered Semiconductor Manufacturing, Freescale Semiconductor, IBM, Innovative Silicon, KLA-Tencor, Lam Research, Magma Design, Nvidia, Samsung, Semico, Soitec, SEH Europe, STMicroelectronics, Symmid Semiconductor, Synopsys, TSMC, Tyndall Institute, UCL (Université Catholique de Louvain) and UMC. Membership is open to all companies and institutions throughout the electronics industry. For more information, see www.soiconsortium.org

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Press Contact: Camille Darnaud-Dufour +33 (0) 6 79 49 51 43 camille.darnaud-dufour@soiconsortium.org

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