



MAJOR SEMICONDUCTOR COMPANIES JOIN FORCES TO LAUNCH DESIGN CHAIN SOLUTION FOR SILICON-ON-INSULATOR TECHNOLOGY

**IBM, ARM and Cadence Collaborate
to Provide Chip and System Designers Access to Key IP**

Boston, MASS., March 23, 2010 – The [SOI Industry Consortium](#) today announced the launch of its “Ready for SOI Technology” program, a global initiative to broaden access to energy-efficient silicon-on-insulator (SOI) technology for the electronics industry. With this program an initial offering of SOI intellectual property has been provided by IBM, ARM, and Cadence Design Systems. More IP has been added by Boeing and Synopsys, with an invitation extended to other developers to add to the growing SOI IP ecosystem.

SOI process technology can provide up to 30 percent chip performance improvement and 40 percent power reduction compared to bulk silicon technology. SOI is widely used today in market leading products found in data centers, offices, vehicles, homes and elsewhere in applications for computing, storage and networking, as well as for graphics-intensive game consoles. The Ready for SOI program is now making necessary design building blocks available to a broader population of chip designers seeking to harness SOI technology’s benefits for new applications, including mobile and consumer products.

A key enabler for this effort is the new SOI Portal hosted on the popular ChipEstimate.com site at www.ChipEstimate.com/SOI. The SOI Portal provides chip designers access to available design building blocks and to the companies supporting chip development on SOI processes.

“ChipEstimate.com has become a critical resource to over 26,000 registered SoC designers by providing central access to over 200 of the world’s largest IP suppliers and foundries,” said Adam Traidman, General Manager at Cadence. “Our new SOI micro-site will serve as an invaluable resource to designers wishing to explore the benefits of SOI technology for their chip design projects.”

To help IP and chip designers transition to SOI, the Ready for SOI program is sponsoring SOI Jump Start Training – [register here >>>](#). This special training event will be hosted by Cadence on April 28, 2010 at the Cadence Engineering Center Auditorium, in San Jose, CA. Jump Start Training will also be available as both a live and recorded webcast.

“We are removing a barrier to industry adoption by giving all chip designers access to the benefits of SOI, not just those working for integrated device manufacturers and high-end ASIC

developers,” said Horacio Mendez, executive director of the SOI Industry Consortium.

“Through the enablement provided by ARM’s SOI libraries and EDA tool suppliers, a vast range of synthesizable IP is now easily portable to SOI technology and physical IP can be readily ported or designed using industry standard tools.”

IBM’s SOI technology with eDRAM is a key enabler for multi-core processors and other integrated circuits and can result in improved systems performance and energy savings for a range of applications including networking, printer, storage, consumer and mobile products.

“IBM was the first company to ship SOI products and we are now in our seventh generation of this leading technology,” said Michael Cadigan, general manager, IBM Microelectronics Division. “Through this collaboration with ARM, Cadence and other suppliers, we are providing an open design system and a proven supply chain to bring the significant performance and power-saving advantages of SOI technology to clients developing mobile and other system-on-chip applications.”

The SOI Industry Consortium invites all chip designers to evaluate the advantages of SOI for their next design by visiting the SOI Portal at www.ChipEstimate.com/SOI. Digital, analog and mixed-signal IP suppliers are invited to participate in listing their offerings on the SOI Portal. Designers worldwide are invited to register and attend the SOI Jump Start training on April 28, 2010 [register now >>>](#), with the option of attending a live event in Silicon Valley hosted by Cadence, or online in a simulcast or recorded webinar.

About the SOI Industry Consortium:

The SOI Industry Consortium is chartered with accelerating silicon-on-insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption. Providing a platform for global collaboration throughout the value chain, the SOI Industry Consortium’s membership includes: AMD, Applied Materials, ARM, Cadence Design Systems, CEA-Léti, Freescale Semiconductor, GLOBALFOUNDRIES, IBM, IMEC, Infotech, Innovative Silicon, Kanazawa Institute of Technology, KLA-Tencor, MEMC, Mentor Graphics, MIT Lincoln Laboratories, Nvidia, Ritsumeikan University, Samsung, Semico, SEH Europe, Soitec, Stanford University, STMicroelectronics, Synopsys, Tyndall Institute, University of California-Berkeley, University Catholique de Louvain, UMC and Varian. Membership is open to all companies and institutions throughout the electronics industry. For more information please visit www.soiconsortium.org.

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