

SOI Industry Consortium's
Ready for SOI Technology
IP Ecosystem Program

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The SOI Industry Consortium is announcing . . .
an important collaboration between major semiconductor
companies to:

1. offer SOI design intellectual property from IBM, ARM, Cadence Design Systems and others
2. make this IP available through a new SOI Portal hosted on the popular ChipEstimate.com (at www.ChipEstimate.com/SOI)
3. invite other companies to participate by offering their IP and services on the SOI Portal to further expand the design ecosystem (already Boeing and Synopsys have joined the effort)
4. offer SOI Jump-Start Training for IP and Chip Designers on April 28, 2010

This is an important step towards the formation of a complete ecosystem to enable designers to take full advantage of the benefits of SOI technology



What kind of IP will be available at the launch?

Nearly 50 foundational IP blocks are initially available, such as:

- Standard cell libraries from ARM, Boeing
- Mixed-signal libraries from Boeing
- Memory compilers (SRAM, register file, eDRAM, ROM, TCAM) from ARM, IBM
- PLLs – IBM,
- General purpose and specialty I/Os from ARM,
- SERDES – IBM, Synopsys
- Data converters (ADC and DAC) from Boeing, Cadence, IBM
- Voltage and temperature sensors from IBM
- Power management kits from ARM

Why is this announcement important? (the story)

Improving power efficiency is top design priority for the semiconductor industry (lower power + higher performance)

To address this priority, SOI process technology has demonstrated up to 30 percent chip performance improvement and 40 percent power reduction compared to bulk silicon technology at the same technology node.

- On October 8, 2009 ARM announced the implementation of ARM's 1176 core in 45nm SOI. Silicon results confirmed these significant performance and power improvement numbers. For a full report please go to:
<http://www.soiconsortium.org/technology-corner>

In addition to power efficiency SOI offers additional benefits:

- improved density and integration
- extended high temperature range
- improved radiation robustness and soft-error rate (SER)



Why is this announcement important? (continued)

Libraries for SOI design using standard EDA tools have been in place since 2009, and as validated in ARM's report, these can be successfully and productively used by design engineers with no prior SOI experience.

In 4Q09 lack of SOI IP became the top remaining barrier for chip designers wanting to adopt SOI.

This announcement means that lack of SOI IP will no longer be a barrier and should give all chip designers access to the benefits of SOI technology.



Ready for SOI Technology program vision:

Build a visible, working IP ecosystem to support SOI adoption in target markets

- IP ecosystem = committed IP, library, EDA tool and design service providers for both physical and soft (synthesizable) IP
- “Visible” = ecosystem is viewable on a mainstream portal used by chip designers
www.ChipEstimate.com selected to host the SOI Portal
- “Working” = **listed** ecosystem suppliers are ready to quote, develop, port, validate and support IP for customer engagements in a response time competitive with existing bulk silicon IP business practices
- Target market collaboration driven within SOI Industry Consortium to accelerate ecosystem expansion



SOI is already used in a variety of products



Ready for SOI Technology program seeks to make available both existing and new SOI IP



About the SOI Industry Consortium

SOI Industry Consortium's mission

The SOI Industry Consortium is a group of leading companies from the electronics industry with the mission of accelerating silicon-on insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption

- The SOI Industry Consortium strives to be the unifying voice of the SOI-based industry
- The SOI Industry Consortium provides its members with a platform for meaningful global collaborations throughout the value chain



The SOI Industry Consortium: A Collaborative Community of 30 Innovation Leaders



Founded October 2007



For more information.....

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