

Questions and Answers on Fully Depleted SOI Technology for next generation CMOS nodes

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abstract

This document is a high level introduction to FD-SOI technology and its applicability to next technology nodes, in the form of a few key questions and their quick answers. No deep technical details are provided here, however Question 15 provides some relevant links.

Short answers are provided first (hypertext links are provided, just click on the question of interest), followed by slightly more detailed answers for the interested readers.

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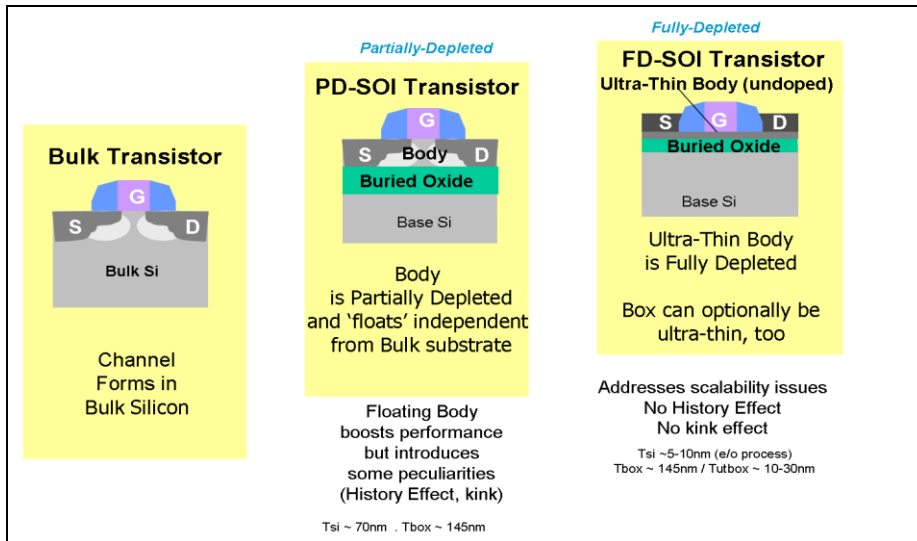
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- Q3- What are the primary application targets of FD-SOI?
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short answers

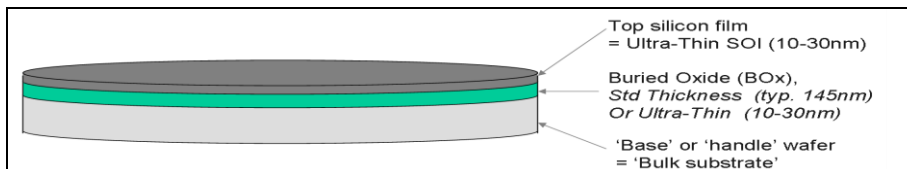
Q1- What is planar Fully Depleted SOI?

A: Planar Fully Depleted Silicon on Insulator (FD-SOI) technology relies on an ultra-thin layer of silicon over a Buried Oxide (commonly called BOx). Transistors built into this top silicon layer are Ultra-Thin Body devices and have unique, extremely attractive characteristics. Two flavors of buried oxide can be used: standard thickness (typically 145nm thick as classically in volume production PD-SOI digital chips today), or ultra-thin BOx, for example 10 or 25nm (UTBOX, Ultra-Thin Buried Oxide).

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FD-SOI Transistors vs. Bulk and PD-SOI Transistors



FD-SOI Starting Wafer

Q2- Why switch to FD-SOI at next CMOS nodes, and what are the key advantages of FD-SOI?

A: FD-SOI solves, with less process complexity, scaling, leakage and variability issues to further shrink CMOS technology beyond 28nm. FD-SOI offers the following major benefits:

- the excellent electrostatic control of the transistor, intrinsic to FD-SOI, acts as a performance booster and enables lower VDD (therefore lower power consumption) whilst reaching remarkable performance,
- FD-SOI strongly reduces the random dopant fluctuation, thus drastically cutting transistor threshold (V_T) variability. In particular, this enables stable, dense, and high-yielding SRAM, functional at very low VDDmin (even in near- or sub-threshold mode with a good SNM),
 - *Simulations and early silicon data predict that, at 22nm node, 6T SRAM macros on FD-SOI could reach 6-sigma yield at VDD as low as 0.5-0.6V* [C Shin et al., UCB, SOI Conference 2009 – K Cheng et al., IBM, IEDM 2009]
- FD-SOI is intrinsically Low Leakage and regains good control of Short Channel Effects. One consequence is the ability to aggressively shrink the gate length, making it easier to fit devices into smaller and smaller pitches and therefore increase logic density to continue Moore's law.

In addition, FD-SOI transistors (which require no halo/pocket implant) natively offer superior analog behavior. This comes with other classical advantages of SOI like much improved Soft-Error Rate, etc.

Conversely, a Bulk approach for next generation technologies is expected to require more and poorer trade-offs in terms of performance vs. static and dynamic power consumption, SRAM stability and yield vs. cell area, process complexity vs. leakage, etc.

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Q3- What are the primary application targets of FD-SOI?

A: They range from high performance, low power Systems on Chip to ultra-low power applications.

This covers markets such as :

- Mobile Internet Devices (Smartphones, Tablets, Netbooks ...),
- Imaging (Digital Camera, Camcorders...),
- Cellular Telecom,
- Mobile Multimedia,
- Home Multimedia (Set Top Box, TV, Blu-Ray),
- Automotive Infotainment,
- etc.

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Q4- Is FD-SOI compatible with cost-sensitive, consumer-type end applications?

A: Yes. FD-SOI efficiently solves the equation: Cost of Ownership (CoO) of the finished Integrated Circuit vs. power, performance, area and manufacturability requirements at the next technology nodes. Some key aspects of the FD-SOI technology (e.g. regarding process complexity, SRAM area/yield trade-off, etc.) have a beneficial impact on the CoO. In addition, optimization programs at Soitec are significantly lowering the cost of SOI as a starting material, with SOI wafer prices expected in the \$500 range per 300mm wafer for high volumes in 2012 (depending on final wafer specifications – ultra-thin Box option, base material requirements, etc.). It is also worth keeping in mind that the contribution of the finished wafer cost to the final CoO of an IC is mitigated by other important die-level aspects like cost of IC packaging, etc.

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Q5- FD-SOI mandates tight wafer specifications : can this be manufactured, who will produce such wafers and when can high volume production start?

A: The thickness of the top silicon layer in starting wafers for FD-SOI is typically 10 – 25nm, with required uniformity within a few Angstroms (6 sigma range less than 1nm). This enables fabrication of planar fully-depleted transistors with only 5-9nm of silicon under the gate. Soitec is already in a position to sample FD-SOI wafers for complete development and qualification of the next CMOS node in line with these tight specifications, and will be ready to deliver high volumes in 2011.

Global capacity for 300mm diameter SOI wafers at Soitec is planned to be of the order of 160 Kwafers/month in 2012. Based on forecasted TAM (Total Available Market) and the anticipated 22/20nm node introduction scenario, this covers estimated market needs until 2014 and can be incrementally increased. In addition, the Smart Cut™ technology used to produce these wafers is also licensed, so multi-sourcing of starting material is possible. Besides, transfer of SOI wafer technology has been successfully demonstrated by transferring thin SOI wafer technology from a manufacturing plant in Bernin, France, to another Soitec manufacturing plant in Pasir Ris, Singapore.

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Q6- Is FD-SOI scalable over several CMOS technology nodes?

A: Yes. Leading papers (VLSI and IEDM conferences, 2008 & 2009) have shown it to be scalable down to the 11nm node at least. This is based on projected requirements in terms of thickness and uniformity of top silicon and BOx for next nodes compared to current quality of FD-SOI wafers.

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Q7- What is the maturity of FD-SOI?

A: FD-SOI CMOS technology is under development at leading edge technology centers (for example, IEDM-2009 provided a snapshot of progress at the IBM Alliance in Albany NanoTech and at ST R&D in Crolles) and is on a path to intercept the 22/20nm node for mainstream Low Power design. Extremely encouraging transistor and RAM bit cell level results targeting the 22/20nm node have been reported, as well as circuit level results in currently available technology, showing FD-SOI is on the right track to meet aggressive 20LP/22LP specifications within the timescales required by the IC industry.

Looking at the overall ecosystem :

- industrial wafers are available (refer to Question 5),
- fab toolsets are the same as those used for Bulk,
- FD-SOI introduces no major disturbance in the design flow (refer also to Question 8). Early design evaluations are ongoing at major R&D centers. Compact models compatible with FD-SOI are on-track for integration into mainstream commercial SPICE simulators. It is anticipated that Design Kit and Library releases would then enable commercial IC design to start in the late 2011- early 2012 timeframe (obviously this will also depend on the resolution of other CMOS challenges, for example scaling of metal interconnects, lithography tools and new rules, etc.).

Therefore, FD-SOI technology has already achieved a very significant maturity versus the schedule of introduction of the next CMOS technology node.

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Q8- Are there any specificities to FD-SOI design, and how about the design ecosystem?

A: There are essentially no specificities to design on FD-SOI. Design will rely on the same flows as Bulk, updated to integrate FD-SOI-capable SPICE compact models. The fundamental work of modeling FD-SOI physics and device structures to build such models has been done. Note that FD-SOI does not exhibit the Floating Body Effect and is free of peculiarities such as history effect (also known as the 1st/2nd switch effect) and kink effect. This makes the porting of designs from bulk to FDSOI very direct.

Overall, developing an FD-SOI design ecosystem for the 22/20nm node is not a daunting task; and in fact is expected to represent a work comparable to enhancing the traditional Bulk CMOS ecosystem to support next generation nodes.

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Q9- Is FD-SOI compatible with low power design techniques?

A: Yes. Virtually all low power techniques currently employed in classical Bulk CMOS technology can be directly ported to FD-SOI. One special case is Body Biasing, which can be very efficiently adapted to FD-SOI in the form of back-plane biasing, using ultra-thin BOx wafers. Besides, VT adjustments are no longer done via doping adjustments as FD-SOI requires no channel doping (which is very advantageous for other reasons): alternative methods exist and are being assessed, including gate stack engineering (same metals as on Bulk and less deviation from mid-gap), back-plane biasing (with ultra-thin BOx) and VDD adjustment.

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Q10- Is it possible to co-integrate FD-SOI and classical Bulk CMOS on the same die?

A: Yes. It is possible to locally etch off the top silicon and the buried oxide to access the Bulk substrate. Using ultra-thin buried oxide wafers, the resulting step height between an SOI zone and a Bulk zone is small enough to be within depth of focus of lithography tools and enable simple co-integration.

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Q11- How about Self-Heating?

A: Self-Heating is not a cause for concern for Low-Power System-on-Chip Design. Experience shows that designers do not need to modify their design style, as self-heating does not jeopardize intended functionality. Its impact on low power circuits is mostly negligible (except possibly for some higher power, DC biased analog devices) and can be accurately taken into account at the SPICE level if wished (selection by simulation switch).

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Q12- How about devices other than logic transistors?

A: Integration of Analog and I/O transistors, with different gate oxides, has been demonstrated on FD-SOI with very good performance. Regarding non-transistor devices: most of them can be ported to ultra-thin SOI either directly or with minor adaptations. For the few of them that pose specific challenges, two approaches exist. One is to do more adaptation work to provide the full device menu on SOI (IBM has been reporting success with this strategy, for example), with the option to locally grow some additional silicon to locally obtain a thicker film. The other is to co-integrate on Bulk the few devices (perhaps some diodes or poly resistors, for example) that are more simply handled that way – as touched on in Question 11.

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Q13- How does planar FD-SOI compare to FinFETs?

A: Both bring rather similar benefits, aiming in particular at regaining good electrostatic control of the transistor. However planar FD-SOI is much more in continuity with planar Bulk, and may be seen as a better benefits vs. manufacturability trade-off than FinFETs.

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Q14- I hear that I_{on} may be a misleading parameter, especially when looking at a Low Power technology – why?

A: I_{on} is a measure of the transistor drive current in static conditions (fixed $V_{gs}=V_{ds}=V_{DD}$) and does not, on its own, completely reflect the maximum operating frequency of circuits. Another key parameter with a significant impact on dynamic performance of Low Power applications is called DIBL (Drain Induced Barrier Lowering). Its impact on switching speed grows as power supply voltage (V_{DD}) reduces, in addition DIBL tends to worsen as gate length shrinks. Therefore, it is important to keep this aspect in mind for Low Power technology scaling.

At equivalent I_{on} , FD-SOI typically provides better performance than a Bulk technology because it exhibits better DIBL. A better parameter than I_{on} to correlate with dynamic performance is I_{eff} (effective current), which includes measurement of the current at different drain-to-source and gate-to-source voltages in its definition.

Now, if looking at performance from the perspective of target I_{off} , the sub-threshold slope is also an important parameter, as it drives the I_{eff} / I_{off} ratio. At equivalent I_{off} , an FD-SOI device will typically have a better I_{on} than a Bulk device because it exhibits a steeper sub-threshold slope; and by virtue of the argument exposed in the former paragraph, even better I_{eff} and dynamic performance.

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Q15- Where can I find more information on FD-SOI?

A: Section “further details” below provides a short selection of articles that give some background on FD-SOI Technology. Many more can be found by checking the references cited in these works. The SOI Consortium (www.soiconsortium.org) is also a valuable source of information. The author of this Q&A can be contacted at xavier.cauchy@soitec.fr and can also help you find out more.

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more details answers

Q1- What is planar Fully Depleted SOI?

A: Planar Fully Depleted Silicon on Insulator (FD-SOI) technology relies on an ultra-thin layer of silicon over a Buried Oxide (commonly called BOx). Transistors built into this top silicon layer are Ultra-Thin Body devices and have unique, extremely attractive characteristics. Two flavors of buried oxide can be used: standard thickness (typically 145nm thick as classically in volume production PD-SOI digital chips today), or ultra-thin BOx, for example 10 or 25nm (UTBOX, Ultra-Thin Buried Oxide).

Some further details:

Note: Other denominations found in the literature include UTB(B) for Ultra-Thin Body (and BOx) and ETSOI for Extra-Thin SOI.

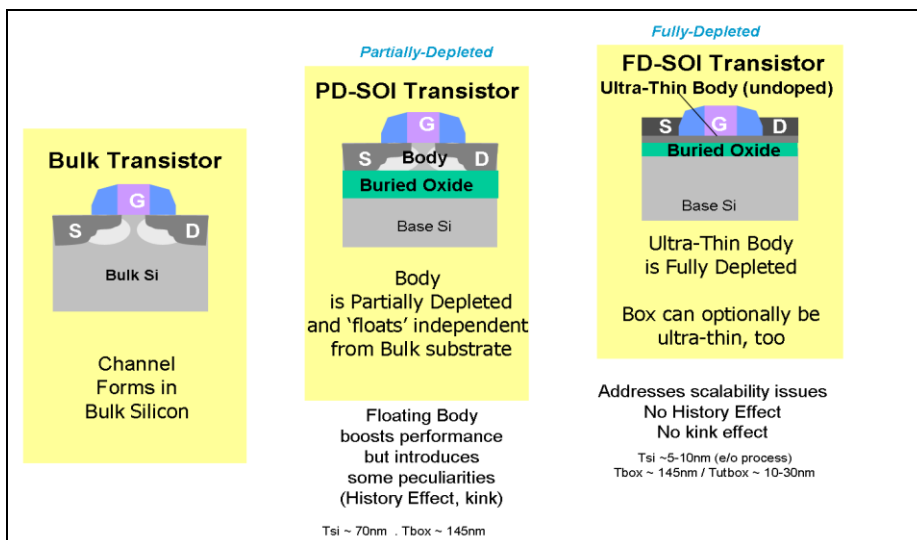
From a physical point of view, the very thin silicon layer enables the silicon under the transistor gate (the body of the transistor) to be fully depleted of charges. The net effect is that the gate can now very tightly control the full volume of the transistor body. That makes it much better behaved than a Bulk CMOS transistor, especially as supply voltage (hence gate voltage) gets lower and transistor dimensions shrink. In addition, FD-SOI does not require doping in the channel.

Use of an ultra-thin BOx may typically be envisaged for some or all of the following reasons :

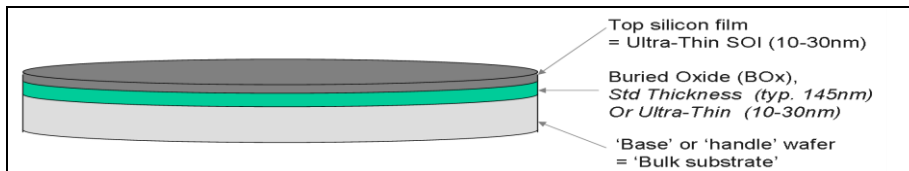
- relaxing of silicon thinness requirements (thus limiting need for a continually thinner transistor body at subsequent CMOS nodes like 16nm-11nm-8nm),
- even better transistor characteristics for some parameters (notably those related to electrostatic control of the channel),
- ability to locally remove top silicon and BOx to reach the base silicon and co-integrate devices on SOI and devices on Bulk, with only a small step (20-30nm) between an SOI zone and an uncovered Bulk zone,
- ability to implant back-planes under the BOx, also to bias them (BOx acting as transistor back-gate). This may be used for shifting VT or for implementing low power design techniques extremely similar to body biasing in Bulk CMOS technologies.

On the other hand, using an ultra-thin BOx comes with a somewhat more challenging process integration scheme.

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FD-SOI Transistors vs. Bulk and PD-SOI Transistors



FD-SOI Starting Wafer

Q2- Why switch to FD-SOI at next CMOS nodes, and what are the key advantages of FD-SOI?

A: FD-SOI solves, with less process complexity, scaling, leakage and variability issues to further shrink CMOS technology beyond 28nm. FD-SOI offers the following major benefits:

- the excellent electrostatic control of the transistor, intrinsic to FD-SOI, acts as a performance booster and enables lower VDD (therefore lower power consumption) whilst reaching remarkable performance,
- FD-SOI strongly reduces the random dopant fluctuation, thus drastically cutting transistor threshold (VT) variability. In particular, this enables stable, dense, and high-yielding SRAM, functional at very low VDDmin (even in near- or sub-threshold mode with a good SNM),
 - *Simulations and early silicon data predict that, at 22nm node, 6T SRAM macros on FD-SOI could reach 6-sigma yield at VDD as low as 0.5-0.6V* [C Shin et al., UCB, SOI Conference 2009 – K Cheng et al., IBM, IEDM 2009]
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In addition, FD-SOI transistors (which require no halo/pocket implant) natively offer superior analog behavior. This comes with other classical advantages of SOI like much improved Soft-Error Rate, etc.

Conversely, a Bulk approach for next generation technologies is expected to require more and poorer trade-offs in terms of performance vs. static and dynamic power consumption, SRAM stability and yield vs. cell area, process complexity vs. leakage, etc.

Some further details:

These characteristics are mostly consequences of using Ultra-Thin Body devices, as these require no channel doping (and therefore do not suffer from Random Dopant Fluctuation, which is rapidly becoming a major problem for Bulk CMOS) and exhibit excellent electrostatic control of the channel. This in turn translates as : excellent VT variability (with record low AVT values reported in [Weber, IEDM2008] and [Cheng, IEDM2009]), low DIBL (Drain Induced Barrier Lowering) –which is a performance boost factor especially at low VDD, limited Short Channel Effects, very good Sub-threshold Slope, and minimum junction capacitance and diode leakage.

In addition, an FDSOI process can be significantly simpler than a Bulk process aimed at the same technology node: the absence of halo doping / pocket implants is an example of simplification, simpler STI (Shallow Trench Isolation) is another one – see for example [K Cheng, IEDM2009] for a list of advantages in the case of the 'ETSOI' flow proposed by IBM.

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Q3- What are the primary application targets of FD-SOI?

A: They range from high performance, low power Systems on Chip to ultra-low power applications.

This covers markets such as :

- Mobile Internet Devices (Smartphones, Tablets, Netbooks ...),
- Imaging (Digital Camera, Camcorders...),
- Cellular Telecom,
- Mobile Multimedia,
- Home Multimedia (Set Top Box, TV, Blu-Ray),

- Automotive Infotainment,
- etc.

Some further details:

In such systems, there is a number of “ad-hoc performance” IP blocks, that need to reach a target frequency to perform their assigned function, but would not take advantage of higher operating frequencies (for example, a USB controller or a video formatting engine): these clearly benefit from the ability of FDSOI to run with remarkable performance and low leakage at low VDD.

There are also some IP blocks that require maximum peak performance --typically embedded processors in high end System on Chips (Mobile Internet Devices for example). These are also addressed, by stretching FDSOI performance through e.g. the use of low VT transistors, forward back-bias, etc. Some often cited challenges to reach high peak performance with ultra-thin body devices have been access resistance reduction and applicability of silicon strain technologies. The good news is that, today, solutions to reach decent access resistance (of the order of 250 ohm.um) on FD-SOI have been demonstrated [Fenouillet ESSDERC2009, Cheng IEDM2009], with more work ongoing and further improvements expected. In addition it has been shown that some strain technology (like CESL) can be used and its effects add up with the electrostatic boost inherent to ultra-thin body [Weber IEDM2008]. Although the total amount of mechanical strain is still lower in ultra-thin body devices than in some Bulk devices, it comes as a bonus to the electrostatic boost which Bulk devices do not enjoy. Interestingly, as technology shrinks, keeping a high efficiency of mechanical strain requires more and more efforts and sophisticated process while, in contrast, the effectiveness of good electrostatic behavior increases naturally. Finally, one additional factor to take into account when considering peak performance is the decreasing effectiveness of (forward) body bias in Bulk vs. the ability to apply efficient and rather large back-bias to FD-SOI devices (through an ultra-thin BOx) [Andrieu VLSI2010].

Besides, most of the applications listed above (especially when they feature peak-performance oriented, power hungry IPs) will enjoy a better effectiveness of several power management techniques they typically use, owing to the FD-SOI benefits mentioned in Q3. Consider for example AVS (Adaptive Voltage Scaling) and Dynamic Voltage and Frequency Scaling (DVFS), as these techniques attempt to set minimum power supply and operating frequency for the ongoing application scenario; or Retention Modes, as they attempt to retain bit cells and some register values at minimum leakage; or Reverse Back Bias (with UTBOx); etc. Finally, much improved variability and matching (as well as absence of history and kink effects) is a big plus for Analog, Mixed Signal and PHY IPs typically found in Systems on Chip.

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Q4- Is FD-SOI compatible with cost-sensitive, consumer-type end applications?

A: Yes. FD-SOI efficiently solves the equation: Cost of Ownership (CoO) of the finished Integrated Circuit vs. power, performance, area and manufacturability requirements at the next technology nodes. Some key aspects of the FD-SOI technology (e.g. regarding process complexity, SRAM area/yield trade-off, etc.) have a beneficial impact on the CoO. In addition, optimization programs at Soitec are significantly lowering the cost of SOI as a starting material, with SOI wafer prices expected in the \$500 range per 300mm wafer for high volumes in 2012 (depending on final wafer specifications – ultra-thin Box option, base material requirements, etc.). It is also worth keeping in mind that the contribution of the finished wafer cost to the final CoO of an IC is mitigated by other important die-level aspects like cost of IC packaging, etc.

Some further details:

Specifically, benefits of FD-SOI that have an impact on CoO include:

- favorable area vs. stability and yield trade-off for SRAMs,
- ability to scale gate length aggressively (benefit of low Short Channel Effects) leading to better logic density and/or less process and integration efforts to fit into a target transistor pitch,
- simplicity of the process, with a potential impact on cost and/or yield,
- less design sign-off margins required, owing to reduced variability,
- potentially lower packaging and cooling cost, owing to lower power dissipation needs,
- etc.

Factoring in these aspects with starting wafer cost and die level costs, the Cost of Ownership of FD-SOI based ICs is expected to be very competitive vs. a (virtual) Bulk counterpart. In any case, the right solution

is probably that which offers, at a reasonable final cost, a competitive power/performance/area/manufacturability trade-off in view of the target applications.

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Q5- FD-SOI mandates tight wafer specifications: can this be manufactured, who will produce such wafers and when can high volume production start?

A: The thickness of the top silicon layer in starting wafers for FD-SOI is typically 10 – 25nm, with required uniformity within a few Angstroms (6 sigma range less than 1nm). This enables fabrication of planar fully-depleted transistors with only 5-9nm of silicon under the gate. Soitec is already in a position to sample FD-SOI wafers for complete development and qualification of the next CMOS node in line with these tight specifications, and will be ready to deliver high volumes in 2011.

Global capacity for 300mm diameter SOI wafers at Soitec is planned to be of the order of 160 Kwafers/month in 2012. Based on forecasted TAM (Total Available Market) and the anticipated 22/20nm node introduction scenario, this covers estimated market needs until 2014 and can be incrementally increased. In addition, the Smart Cut™ technology used to produce these wafers is also licensed, so multi-sourcing of starting material is possible. Besides, transfer of SOI wafer technology has been successfully demonstrated by transferring thin SOI wafer technology from a manufacturing plant in Bernin, France, to another Soitec manufacturing plant in Pasir Ris, Singapore.

Some further details:

The typical SOI thickness of finished devices will be in the 5-9nm range, with starting wafers having a slightly thicker SOI layer, for example 12nm, to allow for some silicon consumption during CMOS processing. Uniformity must be controlled within a few Angstroms to retain the excellent VT stability enabled by undoped channel FD-SOI technology. Soitec offers UTSOI (Ultra-Thin SOI) wafers that fulfill these tight requirements (uniformity measured by standard 41-point ellipsometry), with a UTBOX (Ultra-Thin Buried Oxide) option, and is fully committed to producing these products in very high volumes in line with the IC industry needs.

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Q6- Is FD-SOI scalable over several CMOS technology nodes?

A: Yes. Leading papers (VLSI and IEDM conferences) have shown it to be scalable down to the 11nm node at least. This is based on projected requirements in terms of thickness and uniformity of top silicon and BOx for next nodes compared to current quality of FD-SOI wafers.

Some further details:

Modeling and simulations have indicated future requirements for thickness and uniformity of SOI and BOx and, down to the 11nm at least, they are within the specifications that wafers manufactured for FD-SOI applications are realistically expected to reach [*Weber, IEDM2008 – Andrieu, VLSI2010*]. Actually, it is already possible today to fabricate sample SOI wafers in line with projected requirements for the 11 nm node in FD-SOI technology.

Note that, for device physics reasons, usage of an ultra-thin box relaxes required silicon thinness at the device level. This avoids going below a 5 nm silicon thickness (in the channel) for future nodes – thereby also avoiding possible technological issues.

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Q7- What is the maturity of FD-SOI?

A: FD-SOI CMOS technology is under development at leading edge technology centers (for example, IEDM-2009 provided a snapshot of progress at the IBM Alliance in Albany NanoTech and at ST R&D in Crolles) and is on a path to intercept the 22/20nm node for mainstream Low Power design. Extremely encouraging transistor and RAM bit cell level results targeting the 22/20nm node have been reported, as well as circuit level results in currently available technology, showing FD-SOI is on the right track to meet aggressive 20LP/22LP specifications within the timescales required by the IC industry.

Looking at the overall ecosystem :

- industrial wafers are available (refer to Question 5),
- fab toolsets are the same as those used for Bulk,
- FD-SOI introduces no major disturbance in the design flow (refer also to Question 8). Early design evaluations are ongoing at major R&D centers. Compact models compatible with FD-SOI are on-track for integration into mainstream commercial SPICE simulators. It is anticipated that Design Kit and Library releases would then enable commercial IC design to start in the late 2011- early 2012 timeframe (obviously this will also depend on the resolution of other CMOS challenges, for example scaling of metal interconnects, lithography tools and new rules, etc.).

Therefore, FD-SOI technology has already achieved a very significant maturity versus the schedule of introduction of the next CMOS technology node.

Some further details:

Fully Depleted operation of transistors has been demonstrated in high volume products for years (ultra low-power ICs from OKI, for example), although this was on older lithography. In recent years, the viability of FDSOI as a solution to nanometer CMOS scaling challenges has been demonstrated by leading R&D centers (including LETI, Hitachi R&D, UC Berkeley, etc.). Looking at the near future, competitive and promising FDSOI structures on ultra-thin SOI for the next technology nodes have been reported by a number of major CMOS Technology Development centers, notably IBM, ST, LETI, etc. (see question #15 for some references), although obviously there is still some work to industrialize the 22/20nm FD-SOI solution. From a manufacturing perspective, the FD-SOI process is fully compatible with a Bulk process in terms of CMOS fabrication tooling, does not require any exotic process steps and is actually expected to be simpler than a Bulk process aiming at the same specifications; so these considerations are not threats for getting to a mature FD-SOI process. Wafer readiness and the design ecosystem are also in line with full deployment at 22/20nm, as discussed in questions #5 and #8.

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Q8- Are there any specificities to FD-SOI design, and how about the design ecosystem?

A: There are essentially no specificities to design on FD-SOI. Design will rely on the same flows as Bulk, updated to integrate FD-SOI-capable SPICE compact models. The fundamental work of modeling FD-SOI physics and device structures to build such models has been done. Note that FD-SOI does not exhibit the Floating Body Effect and is free of peculiarities such as history effect (also known as the 1st/2nd switch effect) and kink effect. This makes the porting of designs from bulk to FDSOI very direct.

Overall, developing an FD-SOI design ecosystem for the 22/20nm node is not a daunting task; and in fact is expected to represent a work comparable to enhancing the traditional Bulk CMOS ecosystem to support next generation nodes.

Some further details:

All designers (SoC, IP macrocells, Libraries, Custom Analog, etc.) rely on availability of a Design Platform (Process Design Kit + Design Automation Tools) to work on a given technology node. As soon as such a platform is available, the fact that the underlying technology relies on FD-SOI or Bulk is transparent – given that FD-SOI does not introduce any specific sign-off corners or libraries. In other words, the design and sign-off flow from RTL to chip tape-out will be the same; lower level and custom design flow will not need to be specific either. Direct porting of IPs from Bulk to FD-SOI is possible -- although, for elementary library cells and transistor level designs, even better results may be obtained with specific optimization. More generally those designers that deal with transistor level design may need to be aware of some

details of the technology to finely optimize their design (for example, select the optimal loading of a logic gate for best performance): this is true when switching to any new node, be it Bulk or FD-SOI. As far as development and availability of Process Design Kits and Design Platforms are concerned, the one significant difference versus classical Bulk technology is the development and industrialization of suitable SPICE compact models to represent undoped ultra-thin body transistors (with optional back-bias). Two approaches are proposed today:

- One is to rely on existing SOI compact models to handle such FD-SOI devices. This is what UC Berkeley proposes now, based on the latest BSIMSOI model (BSIMSOI 4.x).
- An alternative solution is to develop a model specific to Undoped Ultra-Thin Body (i.e. Fully Depleted) Transistors, considering that the physics that govern these devices is different from that of Bulk or PD-SOI. R&D centers that have worked on such kinds of models include LETI, UC Berkeley and the University of Florida. These models are closer to the actual physics of the ultra-thin body transistor and may therefore more reliably predict behavior at operating points other than those used to calibrate the model. The next step is to industrialize and integrate these models into commercial SPICE simulators.

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Q9- Is FD-SOI compatible with low power design techniques?

A: Yes. Virtually all low power techniques currently employed in classical Bulk CMOS technology can be directly ported to FD-SOI. One special case is Body Biasing, which can be very efficiently adapted to FD-SOI in the form of back-plane biasing, using ultra-thin BOx wafers. Besides, VT adjustments are no longer done via doping adjustments as FD-SOI requires no channel doping (which is very advantageous for other reasons): alternative methods exist and are being assessed, including gate stack engineering (same metals as on Bulk and less deviation from mid-gap), back-plane biasing (with ultra-thin BOx) and VDD adjustment.

Some further details:

Techniques used at any level above transistor have no sensitivity to whether the technology is based on Bulk or anything else, and therefore are directly usable with designs built on FD-SOI. These include Dynamic Clock Gating, Microarchitectural RTL optimizations, Static and Dynamic Power Switching and Retention Modes, Adaptive Voltage Scaling (AVS), Dynamic Voltage and Frequency Scaling (DVFS). Some of them may actually be more powerful on FD-SOI as noted in Q3.

The few techniques that must be transposed are essentially: body biasing and multi-VT. Forward and reverse body bias are techniques that shift the voltage of the substrate into which bulk transistors are built, to modify the speed/leakage trade-off point of those transistors. An equivalent effect can be obtained with FD-SOI on ultra-thin BOx: much like in Bulk technology, the substrate is contacted to a suitable voltage to bias it under the devices of interest. However with FD-SOI the contacts now go through the BOx, so that the bias is applied to a region just under the BOx and can influence the behavior of the overlying transistors (shifting the speed/leakage trade-off) because the BOx is ultra-thin; *[Andrieu, VLSI2010]* demonstrates this is highly effective. This can also be regarded as a VT modulation and is one way to have multi-VT with undoped channel FD-SOI *[Noel, ESSDERC2009 – Fenouillet, ESSDERC2009]*. Other VT shift techniques include metal gate work function engineering (usable with thick or thin BOx); a combination of both approaches may also make sense. Note that envisaged gate stack engineering approaches do not involve metals other than those now classically used with High-K Metal Gates on Bulk; in fact engineering may be simpler as there is no need to reach the band edges.

Finally, channel length modulation techniques (for selective leakage reduction or higher-VT devices) are still usable with FD-SOI technology, however it must be kept in mind that the VT roll-off will normally be less pronounced than in a Bulk technology counterpart, owing to the excellent electrostatic behavior of FD-SOI devices: this may influence the impact of those techniques.

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Q10- Is it possible to co-integrate FD-SOI and classical Bulk CMOS on the same die?

A: Yes. It is possible to locally etch off the top silicon and the buried oxide to access the Bulk substrate. Using ultra-thin buried oxide wafers, the resulting step height between an SOI zone and a Bulk zone is small enough to be within depth of focus of lithography tools and enable simple co-integration.

Some further details:

Using an ultra-thin Box, the resulting step between an SOI region and a Bulk region is about 20-35nm. Structures kept on Bulk might for example be those that are less straightforward on ultra-thin SOI like ESD protections, or perhaps some specific, more complex IP blocks that designers prefer to keep on Bulk for any reason (legacy etc.) – assuming a Bulk implementation is compatible with the needs of such IPs. A process that co-integrates Bulk devices and FD-SOI devices is a little more costly than a pure FD-SOI technology; however because many process steps can be shared the overhead can be very reasonable – and can be even lower if using co-integration for very simple structures only, such as bulk diodes for example. Refer for example to [Fenouillet, IEDM2009].

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Q11- How about Self-Heating?

A: Self-Heating is not a cause for concern for Low-Power System-on-Chip Design. Experience shows that designers do not need to modify their design style, as self-heating does not jeopardize intended functionality. Its impact on low power circuits is mostly negligible (except possibly for some higher power, DC biased analog devices) and can be taken into account at the SPICE level if wished (selection by simulation switch).

Some further details :

One concern sometimes expressed about SOI is self-heating: the presence of buried oxide could make the temperature of the channel rise more than in a classical transistor on Bulk, especially in the case of continuous current flow (e.g. in analog biasing circuits).

However, examining practices of designers that do have SOI experience, it appears that, as far as low power design is concerned, this is more a fear than an actual threat. They do not modify their design practices for self-heating concern; simply, if wished (option turned on), SPICE models can model this effect and take it into account to make sure the simulations used to validate transistor level design accurately represent the silicon's behavior.

Reasons invoked to explain why self-heating is not a practical threat include:

- Channel self-heating also exists in Bulk – the BOx would increase it to some extent,
- The time constant associated to local temperature rise is such that its effect is not a concern for switching logic,
- A significant proportion of the heat generated (both in Bulk and SOI) would be quickly conducted by metal connections to the top side of the chip and package (depending on packaging scheme, transistor dimensions etc.); and BOx has no impact on this mechanism;
- At a more global scale (block or die-level), the lower thermal conductivity of the SiO₂ BOx beneath the transistors (lower than Si by 2 orders of magnitude) must be put in perspective with the ratio of BOx thickness (typically, 10nm for Ultra-Thin to 145nm for thicker BOx) to finished wafer thickness (several tens of microns) : thermal insulation of the BOx is relatively small (case of standard BOx) to negligible (case of UTBOX) compared to the thermal insulation due to the Si substrate itself. In other words, evacuation of heat towards the bottom side of a finished wafer is not so much easier without a Box than with a BOx. This rationale is a little simplistic as interface and other nanostructure effects must be taken into account in a more rigorous analysis, but is an interesting first order.

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Q12- How about devices other than logic transistors?

A: Integration of Analog and I/O transistors, with different gate oxides, has been demonstrated on FD-SOI with very good performance. Regarding non-transistor devices : most of them can be ported to ultra-thin SOI either directly or with minor adaptations. For the few of them that pose specific challenges, two approaches exist. One is to do more adaptation work to provide the full device menu on SOI (IBM has been reporting success with this strategy, for example), with the option to locally grow some additional silicon to locally obtain a thicker film. The other is to co-integrate on Bulk the few devices (perhaps some diodes or poly resistors, for example) that are more simply handled that way – as touched on in Question 11.

Some further details:

Non-transistor devices required for SoC integration fall in two categories :

- devices that do not involve the Bulk substrate, for example inter-metal capacitors,
- devices that do involve the Bulk substrate, for example some diodes.

Porting the first category to FD-SOI is straightforward.

Some devices of the second category can also be easily ported to ultra-thin film FD-SOI, because they simply rely on usage of “active” silicon, and thin film is not a problem. Also, a device for which thin film is a problem may sometimes be replaced by an alternative structure to achieve the same goal. Where extreme silicon thinness is a problem and no satisfactory alternative structure can be identified, then there is the option to locally grow silicon to increase its thickness (and perhaps reuse PD-SOI like structures), or to locally etch off top silicon and Buried Oxide, thus giving access to the underlying Bulk substrate and so a classical Bulk CMOS structure can be kept (hybrid Bulk-FDSOI co-integration).

[Fenouillet, IEDM2009] and [Cheng, IEDM2009] report some results of Analog and I/Os on ultra-thin SOI.

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Q13- How does planar FD-SOI compare to FinFETs?

A: Both bring rather similar benefits, aiming in particular at regaining good electrostatic control of the transistor. However planar FD-SOI is much more in continuity with planar Bulk, and may be seen as a better benefits vs. manufacturability trade-off than FinFETs.

Some further details:

The FinFET is actually a Fully Depleted Technology, too, and the motivations to go to FinFET or planar FD-SOI are similar : essentially the objective is to drastically improve electrostatic control.

In theory, FinFETs have the added advantage of offering better density and slightly better electrostatics (although some argue that this is still to be achieved experimentally). However, in order to live up to its promises, FinFETs are faced with the challenges of a disruptive approach that requires mastering technological processes compatible with tri-dimensional geometries (in terms of doping, etching...) and minimizing the variability of the transistor width (which is roughly as influent as the gate length on the FinFET characteristics). The conclusion therefore depends on how process complexity and manufacturability are weighted, however planar FD-SOI is clearly an appealing solution.

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Q14- I hear that I_{on} may be a misleading parameter, especially when looking at a Low Power technology – why?

A: I_{on} is a measure of the transistor drive current in static conditions (fixed $V_{gs}=V_{ds}=V_{DD}$) and does not, on its own, completely reflect the maximum operating frequency of circuits. Another key parameter with a significant impact on dynamic performance of Low Power applications is called DIBL (Drain Induced Barrier Lowering). Its impact on switching speed grows as power supply voltage (V_{DD}) reduces, in addition DIBL tends to worsen as gate length shrinks. Therefore, it is important to keep this aspect in mind for Low Power technology scaling.

At equivalent I_{on} , FD-SOI typically provides better performance than a Bulk technology because it exhibits better DIBL. A better parameter than I_{on} to correlate with dynamic performance is I_{eff} (effective current), which includes measurement of the current at different drain-to-source and gate-to-source voltages in its definition.

Now, if looking at performance from the perspective of target I_{off} , the sub-threshold slope is also an important parameter, as it drives the I_{eff} / I_{off} ratio. At equivalent I_{off} , an FD-SOI device will typically have a better I_{on} than a Bulk device because it exhibits a steeper sub-threshold slope; and by virtue of the argument exposed in the former paragraph, even better I_{eff} and dynamic performance.

Some further details:

I_{on} is a measure of the transistor drive current at fixed $V_{gs}=V_{ds}=V_{DD}$. However the propagation time through a logic gate depends on the current that effectively flows during a logic transition, that is with evolving voltages at the terminals of the transistors involved. Therefore, on its own, I_{on} does not completely

correlate with dynamic performance (i.e. maximum operating frequency). Another key parameter impacting performance of a low power technology is the Drain Induced Barrier Lowering (DIBL), because it impacts the drain current that will effectively flow along time as a logic gate switches; performance improves as DIBL reduces. The impact of DIBL on performance grows as the difference between VDD (power supply) and VT (threshold voltage) reduces. This explains why a technology that must combine low operating power (with low VDD) and low or reasonable leakage (with limited use of low VT transistors) is very sensitive to DIBL. A complete explanation can be found in [Skotnicki, IEDM2009 Short Course 'Low Power Logic and Mixed Signal Technologies'].

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Q15- Where can I find more information on FD-SOI?

A: Section "further details" below provides a short selection of articles that give some background on FD-SOI Technology. Many more can be found by checking the references cited in these works. The SOI Consortium (www.soiconsortium.org) is also a valuable source of information. The author of this Q&A can be contacted at xavier.cauchy@soitec.fr and can also help you find out more.

Some further details:

Ultra-thin FD-SOI Technology:

- "Non-classical MOSFET solutions for power-efficient CMOS",
A. Thean (Freescale), EETimes-India, Dec.2006 (eetindia.com)
- "Low Power Logic and Mixed Signal Technologies",
T. Skotnicki (ST), IEDM2009 Short Course
- "Fully Depleted Extremely Thin SOI Technology Fabricated by a Novel Integration Scheme Featuring Implant-Free, Zero Silicon Loss, and Faceted Raised Source Drain",
K. Cheng and al. (IBM), Symposium on VLSI Technology, June 2009
- "Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications",
K. Cheng and al. (IBM), IEDM 2009
- "High Immunity to Threshold Voltage Variability in Undoped Ultra-Thin FDSOI MOSFETs and its Physical Understanding",
O. Weber et al. (LETI), IEDM 2008
- "Hybrid FDSOI/Bulk high-k/Metal Gate Platform for Low Power (LP) Multimedia Technology",
C. Fenouillet-Beranger et al. (ST-LETI), IEDM 2009
- "Low Leakage and Low Variability Ultra-Thin Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond"
F. Andrieu et al. (LETI), Symposium on VLSI Technology, June 2010
- "Forecasted Impact of Fully Depleted SOI Technology on Design",
X. Cauchy (Soitec), 2009, upon request

Back-biasing techniques:

- "Silicon on Thin Box (SOTB) CMOS for Ultralow Standby Power with Forward-biasing Performance Booster",
T. Ishigaki et al. (Hitachi), Solid State Electronics, Vol.53
- "Robust Multi-VT 4T-SRAM Cell in 45nm Thin Box Fully Depleted SOI Technology with Ground Plane",
JP Noel et al. (LETI), IC-ICDT 2009
- "Impact of a 10nm Ultra-Thin BOx (UTBOX) and Ground Plane on FDSOI devices for 32nm node and below",
C. Fenouillet-Beranger et al. (ST-LETI), ESSDERC 2009
- "A Simple and Efficient Concept for Setting UP Multi-VT Devices in Thin Box Fully-Depleted SOI Technology", FDSOI device
JP Noel et al. (ST-LETI), ESSDERC 2009

FD-SOI SRAMs:

- “SRAM Yield Enhancement with Thin-BOX FD-SOI”,
C Shin et al. (UC Berkeley), SOI Conference, 2009
- “Low Voltage ($V_{dd} \sim 0.6V$) SRAM Operation Achieved by Reduced Threshold Voltage Variability in SOTB (Silicon on Thin Box)”,
R. Tsuchiya et al. (Hitachi), Symposium on VLSI Technology, June 2009

Plus - a little more dated but still interesting:

- Book “Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications”,
T. Sakurai, A Matsuzawa, T Douseki, Springer, 2006

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