Comparison Between Analog Performance of Standard and Strained Triple-Gate nFinFETs

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1. Abstract

This work shows a comparison between the analog performance of standard and strained Si (sSOI) n-type triple-gate FinFETs with high-κ dielectrics and TiN gate material. Different channel lengths and fin widths are studied. It is demonstrated that both standard and strained FinFETs with short channel length have similar analog properties whereas the increase of the channel length degrades the Early voltage of the strained devices, consequently decreasing the device intrinsic voltage gain.

2. Introduction and Device Fabrication

The FinFET is a promising device structure for the sub-100 nm CMOS era due to the excellent gate control of the channel charges allowing for excellent short-channel immunity.

The use of process-induced mechanical strain demonstrated improvements of the carrier mobility leading to higher current drive without penalties in off-state current. The use of biaxially strained material (or sSOI) is one of the possible techniques to obtain a strained silicon layer.

In this work we studied triple-gate nFinFETs fabricated on SOI wafers with 145 nm buried oxide thickness according to the process described in ref. [1]. The top silicon layer thickness (which is the fin height -H_{Fin}) is 60 nm and 55 nm for standard and sSOI FinFETs, respectively. After the silicon film definition a 1 nm thick interfacial thermal oxide is grown followed by the deposition of 2 nm HfO_2. A 5 nm thick TiN layer is then deposited and 100 nm thick polysilicon capping completes the gate stack. No channel doping or halo implantation is applied during the processing. Nickel silicidation is used in all device electrodes. Following the same process flow devices are fabricated on a sSOI wafer with 1.5 GPa intrinsic biaxial tensile strain.

3. Results and Discussion

The impact of strained material adoption on the performance of FinFETs is initially verified by looking at the maximum transconductance ($g_{m,max}$) in linear region (V_{DS}=50 mV) as a function of the fin width (W_{Fin}) for single fins ranging from 20 nm to 870 nm with channel length (L) of 10 µm. The percentage improvement on $g_{m,max}$ (and hence on the carrier mobility) decreases from about 75% for W_{Fin}=870 nm to 56% for W_{Fin}=20 nm. For the wider fin the conduction occurs mainly at the top in the (100) plane whereas for the narrow one the (110) plane in the sidewalls is dominating. This result indicates a dependence on the crystalline orientation with of the carrier mobility improvement provided by the strained material, as demonstrated in ref. [2]. As demonstrated in ref. [1] the reduction on W_{Fin} transforms the strain from biaxial to uniaxial, affecting the $g_{m,max}$ gain. Also the series resistance (R_S) is higher for the narrow sSOI FinFETs due to the smaller H_{Fin}.

The dependence on the channel length has been verified for multiple fin structures composed by 30 parallel fingers with W_{Fin}=20 nm at V_{DS}=0.1 V, as presented in fig. 1.

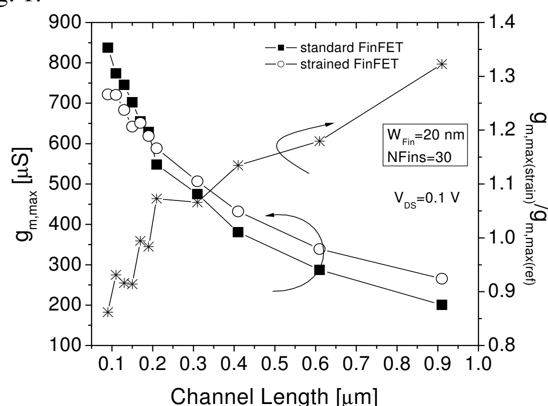

Fig. 1 – *Measured $g_{m,max}$ as a function of L at V_{DS}=0.1V for FinFETs with W_{Fin}=20 nm.*

It is clear from fig. 1 that the use of strained material only results in better transconductance (and hence mobility) for devices longer than 0.20 µm. This reduced $g_{m,max}$ enhancement at shorter L can attributed to the non-scalability of R_S [3]. The improvement on $g_{m,max}$ of strained FinFET increases with L up to 1.33 for 0.91 µm long transistors.

In order to compare the analog properties of both FinFETs the Early Voltage ($V_{EA} \approx I_{DS}/g_{DS}$, I_{DS} being the drain current and g_{DS} output conductance) has been

evaluated as a function of W_{Fin} for single fins of L=10μm biased at a gate voltage overdrive (V_{GT}=V_{GS}-V_T, V_{GS} is the gate voltage and V_T is the threshold voltage) of 0.2 V and V_{DS}=0.6 V, as presented in fig. 2. As for the $g_{m,max}$ the V_{EA} is also influenced by a W_{Fin} reduction. For W_{Fin} wider than 370 nm the V_{EA} is larger in strained FinFETs whereas for narrower fins the V_{EA} can become about 4 times smaller than for standard FinFET at W_{Fin}=20 nm. Using the extracted values for g_m and g_{DS} at V_{GT}=0.2 V and V_{DS}=0.6 V the voltage gain (A_V=g_m/g_{DS}) has been calculated and the results are also plotted in fig. 2. The W_{Fin} reduction causes a degradation on A_V if compared to the results for standard FinFET. On the other hand, wider strained FinFETs overcome the A_V of standard one.

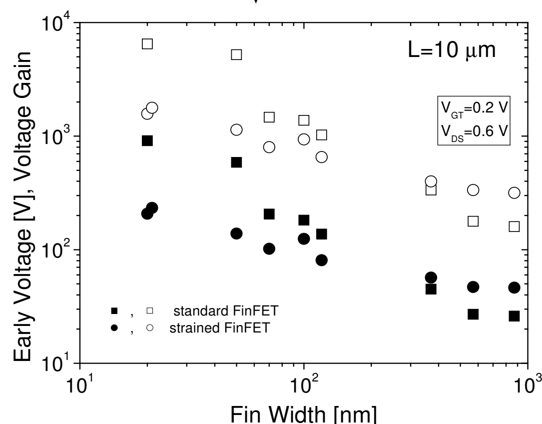

Fig. 2 – *Measured Early Voltage and Voltage Gain as a function of W_{Fin} at V_{GT}=0.2 V and V_{DS}=0.6 V. Closed symbols refer to V_{EA} and opened symbols to A_V.*

The variation of V_{EA} and A_V with L for multiple fins with W_{Fin}=20 nm is presented in fig. 3, also at V_{GT}=0.2 V and V_{DS}=0.6 V.

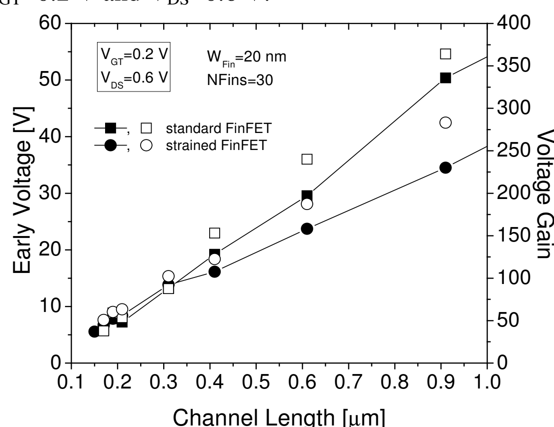

Fig. 3 – *Measured Early Voltage and Voltage Gain as a function of L at V_{GT}=0.2 V and V_{DS}=0.6 V for multiple fin structure with W_{Fin}=20 nm and 30 parallel fins. Closed symbols refer to V_{EA} and opened symbols to A_V.*

As the channel length increases, the effect of strain becomes more pronounced and starts degrading V_{EA} with respect to standard FinFETs. This effect is in agreement to what is presented in fig. 2, where long-channel narrow FinFETs presented reduced V_{EA} compared with standard ones, independently if single or multiple fingers are considered, undermining the influence of R_S as the multiple fingered structures have reduced R_S. For shorter L, as the effect of strain practically disappears, the V_{EA} becomes similar. Following the same tendency given by V_{EA}, the A_V is nearly the same for shorter devices. On the other hand, for longer devices the A_V of standard FinFET overcomes the results for strained ones by more than 30%. Notwithstanding the strained FinFET presents better g_m the degradation demonstrated in fig. 3 for V_{EA} results in an increase of g_{DS} that overcomes the benefits of g_m leading to worst A_V. On the other hand, for narrow FinFETs the effect of strain is favorable to both g_m and g_{DS}, resulting in larger A_V than in standard FinFETs.

Following ref. [4] the measured V_{EA} depends on the intrinsic device Early Voltage (V_A), the series resistance and the carrier mobility. On the other hand, the V_A depends mainly on Drain Induced Barrier Lowering (DIBL). In both types of structures under investigation, with single or multiple fingers, the R_S is nearly the same for standard and biaxially strained FinFETs. In order to evaluate the possible parameters affecting the differences of V_{EA} expressed in figs. 2 and 3 the inverse subthreshold slope (S) and DIBL parameters were extracted for L=0.21 μm and 0.91 μm. In both cases the S and DIBL are quite similar when changing from standard to strained devices. The S (extracted with V_{DS}=0.05 V) decreases from 64 mV/dec. to 62 mV/dec. and DIBL (V_{DS}=0.1 V and V_{DS}=0.6 V) decreases from about 10 mV/V to 3 mV/V when increasing L. The combination of these results ensures that no short-channel effects are taking place. This suggest the degradation of V_A for narrow FinFETs induced by the application of strain is the cause of V_{EA} degradation.

4. Conclusions

A comparison between the analog performance of FinFETs made in standard material and biaxially strained substrates has been reported. Independently of the W_{Fin} under study, the presence of strain in long-channel transistors is effective to improve the carrier mobility. On the other hand, the narrower strained FinFETs presented a degradation of the Early Voltage with respect to standard FinFETs. This degradation is only observed for longer devices, where the effect of biaxially strain is more effective. Although the transconductance improvement is larger for longer devices, the associated degradation of the ouput conductance (and hence Early Voltage) degrades the voltage gain. Shorter devices present similar Early Voltage and voltage gain as the effect of strain is nearly absent on these devices.

References

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