

DC and RF characteristics of FinFET over a wide temperature range

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1. Abstract

DC and RF characteristics of n-type FinFET transistor over a wide temperature range, from 77 to 473K, are presented for the first time. We experimentally demonstrate that the impact of temperature on the main analog and RF factors of merit of FinFETs is similar to what it can be observed for classical deep submicron single gate MOSFETs.

2. Introduction

In recent years, FinFET transistors have received much interest thanks to the better immunity to short-channel effects [1]. DC characteristics of FinFETs at high temperature were recently reported in [2]. RF characteristics of Bulk Si MOSFETs measured at low temperature (77K) have been presented in a few papers [3]-[4]. To the knowledge of the authors, the DC and RF characteristics, over a wide temperature range, of advanced MOSFETs such as FinFETs have not been reported in the literature yet. This is the aim of the present paper.

3. Device Description

Triple gate multifingered, 60-nm channel length, n-type FinFET, with 50 gate fingers and 9 fins per finger, is characterized. The fin width and height are of 32 and 60 nm, respectively. The device is fabricated on top of a 145 nm buried oxide. The gate stack includes 2 nm CET (Capacitance Equivalent Thickness) SiON, 5 nm MOCVD TiN metal gate and 100 nm-thick polysilicon. The channel is left undoped and HALOs are not implanted. Two measurement setups are used to perform the DC and RF characterization of the device under test: a cryogenic probe station for temperatures ranging from 70-300K and a high temperature chuck mounted with a classical RF probe station for the measurements of DC and high frequency parameters from 300-473K range.

4. DC and RF Characterization

Fig. 1 shows the threshold voltage (V_T) and the DC gate transconductance G_m as a function of temperature for a 60-nm n-type FinFET. As the temperature increases, the intrinsic concentration of mobile carriers (n_i) in the transistor channel increases leading to a reduction in the gate voltage needed to reach the strong inversion regime

and then causing a linear reduction of V_T as observed in Fig. 1. For the transconductance G_m , its reduction with the temperature increase is mainly due to the mobility degradation. For bulk Si MOSFETs V_T^{77K}/V_T^{300K} ratios of 1.3 and 1.2 for 0.18 μm and 65 nm channel length, respectively, were observed in [3]-[4]. For 60 nm FinFET the ratio is of 1.4 for the temperature range (77/300K) and 2.4 for the temperature range 77-473K. Furthermore, the peak G_m^{77K}/G_m^{300K} ratio, in saturation was about 1.5 for both Si bulk transistors in [3]-[4] while it is 1.56 for FinFET in the same temperature range, and 2 for 77-473K range. Fig. 2 shows the subthreshold slope (S) as a function of temperature for a 60 nm FinFET. The measured S^{77K}/S^{473K} ratio is of approximately 0.33. Similar value has been obtained for Si Bulk MOSFET [3]-[4] from measurements made at low temperature.

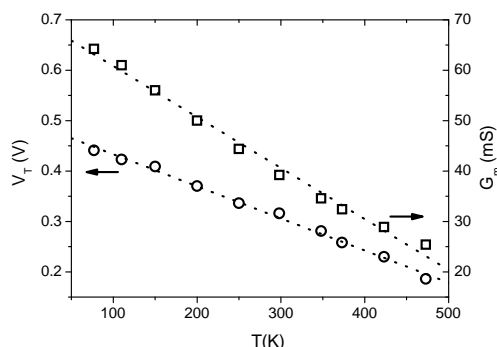


Fig. 1: V_T and G_m as a function of temperature. G_m is measured at $V_{DS}=1.1$ V and $V_{GS}-V_T=0.2$ V.

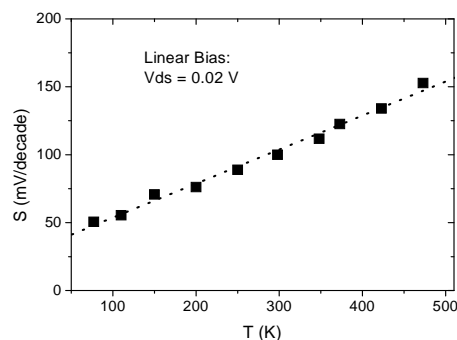


Fig. 2: Subthreshold slope as a function of temperature.

For the RF characterization, S-parameters are measured from 40 MHz to 65 GHz at various temperature conditions, from 77K to 473K. The coplanar pads and feed lines are withdrawn using on-wafer de-embedding

structures including an open test structure. Based on the small-signal equivalent circuit presented in Fig. 3 and specific extraction techniques [5]-[6], the intrinsic and extrinsic parameters are extracted for various temperatures. The extrinsic resistances were obtained in strong inversion ($V_{DS}=0$ V and various $V_{GS} > V_T$), by linear regression of Z-parameters vs. $1/(V_{GS}-V_T)$ [6]. Fig. 4 shows the extracted resistances as a function of temperature. R_d and R_s slightly increase with the temperature. As temperature increases the mobility is degraded, incrementing resistivity of the implanted and LDD regions. On the contrary, R_g is reduced as temperature increases, which could be related to a carrier mobility increment in the poly-Si region [7], or metal/Poly-Si interface effects, or even to an artefact of the extraction technique itself. Further investigations are needed to clarify this behaviour. After withdrawing the extrinsic resistances, the intrinsic parameters are extracted [5] in saturation ($V_{DS}=1.1$ V and $V_{GS}=0.62$ V). Figs. 5 and 6 show the extracted intrinsic transconductance (G_{mi}), output conductance (G_{dsi}) and capacitances, respectively. Fig. 7 shows the unit gain current frequency (f_t). It is worth noting that the intrinsic capacitances (C_{gsi} and C_{gdi}) in Fig. 5 are almost constant over the whole temperature range.

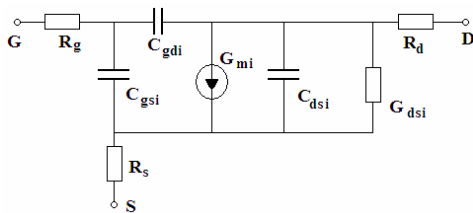


Fig. 3: Equivalent circuit used for the parameters extraction. R_g , R_d and R_s represent the extrinsic series resistances.

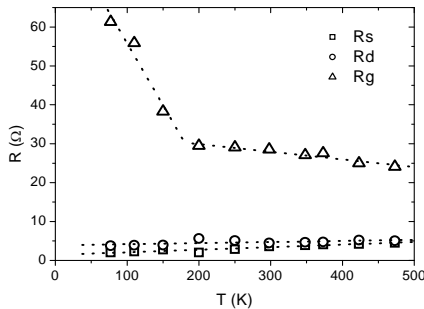


Fig. 4: Extrinsic series resistances vs. temperature.

Fig. 6 indicates the decrease of G_{dsi} and G_{mi} with temperature increase. The conductance reduction is related to mobility degradation. From Fig. 6, $G_{mi}^{77K}/G_{mi}^{300K}$ ratio is 1.5 and 1.9 for 77-473K range. For comparison purpose, $G_{mi}^{77K}/G_{mi}^{300K}$ ratios of 1.4 and 1.3 for 0.18 μm and 65 nm bulk transistors, respectively, are given in [4]-[5]. Finally, in Fig. 7 a 77/300K ratio of 1.3 on f_t is observed, which corresponds to an increment of 33%. Similar f_t enhancement has been reported in [3] for 65-nm Si Bulk MOSFET. At high temperature, the 300/473K f_t ratio of 60-nm FinFET shows the same value of 1.3, corresponding to a decrement of 23%. Recently, a cutoff

frequency reduction of 21% has been measured for 130 nm Partially-Depleted SOI transistors [8]. f_t is directly related to G_{mi} variation versus temperature.

5. Conclusions

DC and RF parameters of a 60-nm FinFET are presented for a wide temperature range. The DC parameters show a strong thermal dependence, whereas for RF parameters, the intrinsic capacitances are nearly constant, and G_{dsi} and G_{mi} are temperature dependent. f_t shows an increment of 33% from 300 to 77K and a reduction of ~23% from 300 to 473K. The overall results show that FinFETs have a similar thermal behavior respectively to bulk and SOI technologies.

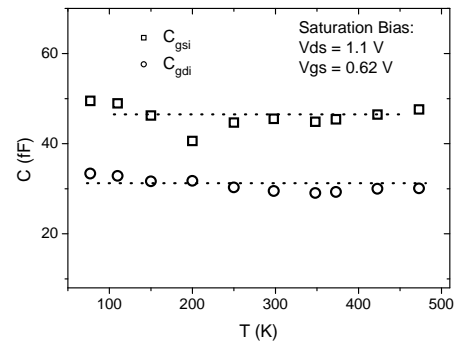


Fig. 5: Intrinsic capacitances vs. temperature.

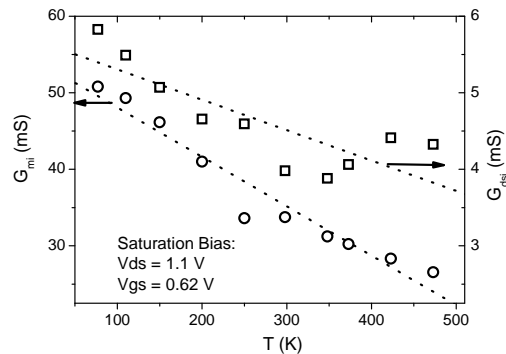


Fig. 6: Intrinsic G_{mi} and G_{dsi} vs. temperature.

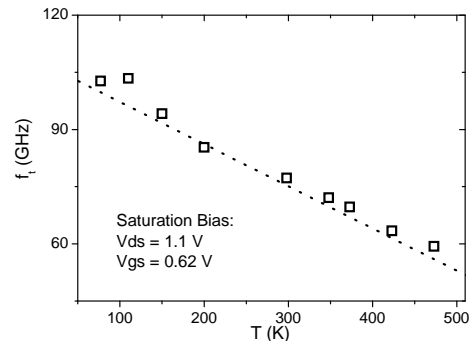


Fig. 7: f_t vs. temperature.

References

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