



www.soiconsortium.org

SOI implementation guide

SOI circuit design overview

By **Nghia Phan**

Distinguished Engineer, IBM Systems and Technology Group, Rochester - MN

nphan@us.ibm.com

SOI implementation guide

SOI circuit design overview

By Nghia Phan

Distinguished Engineer,

IBM Systems and Technology Group

Total chip power, both DC/AC, have been and increasingly will continue to be one of the major issues facing designers. Focus on power is being driven by increases in device leakage and the exponential growth in the number of transistors per design resulting from technology scaling. In addition, isolation scaling in bulk beyond the 32nm node will likely result in bulk process complexity not present in SOI therefore narrowing or reversing the SOI/bulk cost differential. For these reasons, interest in SOI as an alternative to bulk technologies is accelerating.

This article will address the partially depleted SOI circuit design advantages such as improved chip performance and lower power consumption as well as design issues which have been on the mind of CMOS bulk circuit design community.

advantages and design issues

SOI has many well know advantages over bulk technologies. Improved chip performance due to lower junction capacitance, floating body, and improve short channel effect, significantly better SER immunity and the elimination of latch up as a design concern are all clear SOI advantages. But for much application, improved power will be most interesting to designers.

However, there are three main unique SOI circuit design issues due to floating body and the insulation layer of the SOI wafer that bulk circuit designers do not have to deal with.

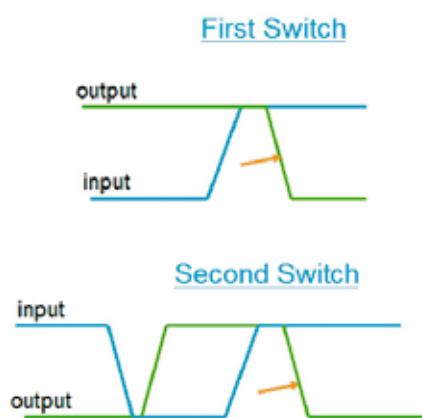
1. history effect

The body of the nfet or pfet in the SOI wafer is floating instead of tie to ground (nfet) or vdd (pfet) as in the bulk CMOS. This floating body can change the FET threshold due to differences in the body voltages. This could cause variation in the circuit delay and mismatch between two identical devices. As the SOI circuit switches, the body voltages of the switching transistors will change from their previous steady state condition. This is called the history effect. This is one of the most interesting circuit design issues in SOI but it is also a benefit of SOI which contributes to SOI performance advantage over bulk CMOS. Learning how to model and predict the body voltage of the SOI transistors will lead to a successful SOI circuit design.

A SOI logic circuit can have different (faster) delay if switching regularly verses a circuit that has been inactive for a long time and then switches. If a circuit is not active for long enough time to be in a steady state and then switches, this switching activity is called first switch. If the circuit is switching more regularly, this is called second switch (Figure 1). Typically, second switch has faster delay than first switch due to the body to source voltage of the second switch is higher than first switch which lowers the V_t of the second switch transistor.

- **Digital static CMOS circuit:** There are no real functional concerns due to history effect. The same circuit designed to work in bulk can be used for SOI without any modifications. The main difference is in the timing model methodology. The following methodologies can be used to simplify the process of generating the timing model of SOI static CMOS circuits.

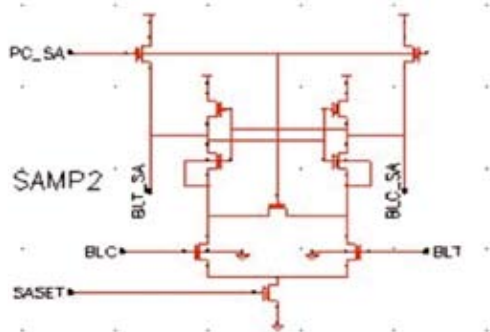
Figure 1. First switch/Second switch definitions



- **Average body voltage method:** This method calculates the average body voltage during switching with various loads and frequencies, and applied that voltage to the switching device to generate the delay used by the timing model. This method is very complicated and takes longer simulation time since the body voltage needs to be calculated a head of time and applied to the Spice simulation during the circuit characterization. However this method can predict chip performance closer to the actual hardware.

- **First switch, second switch method:** With this methodology, the first switch condition is used to create the timing model for the circuit to be used by the slow path delay to predict the maximum frequency of the design. The second switch condition is used to create the timing model for the circuit to be used by the fast path delay to predict race condition. This method generally will under predict the design performance but the timing model is much simpler and easier to create.

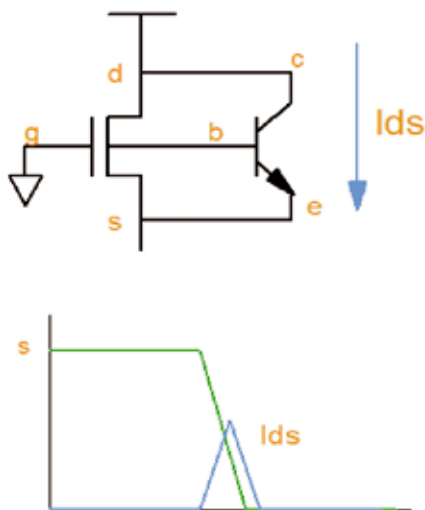
Figure 2. Body contact tie to ground on SRAM sense amp



• **SRAM sense amplifier:** Typical SRAM design uses a sense amp to sense the voltage of the bit cell. This requires matching transistors to properly sense the signal of the bit cell. Due to history effect, these sensing transistors can have different body voltages and create mismatch between them. To address this type of design issue, SOI technology provides other type of transistors such as the body contact transistors. The body contact transistors have one additional terminal to provide the circuit designers option of connecting the body to any nodes in their designs. One common usage is to tie the body to ground (nfet) or Vdd (pfet) to reduce or eliminate the history effect. In this case, the SOI transistors behave similar to bulk transistors. The negative effects of the body contact transistors are that they are about two times larger and switching slower than the floating body transistors. Therefore, it is recommended to use body contact transistors only in places that required for the functionality of the circuit designs. To eliminate the mismatch in the SRAM sense amplifier, the body contact transistors are used on the sensing transistors of the SOI SRAM sense amplifier design (Figure 2).

• **Analog and IO designs:** On a device operating as an “analog” transistor, a body contact may be needed. Without a body contact, the potential of the body will float to a value which is dependant upon the biases applied to the gate, source and drain contacts, and will also become a function of time, impacting output resistance of the device and its Vt-matching to the next device. The electrical behavior of SOI transistors can be significantly different from bulk transistors because of floating body effects. In typical analog designs, body contact transistor can be used as the current source or any matching transistors designs to eliminate the floating body effect.

Figure 3. Bipolar current of the SOI FET



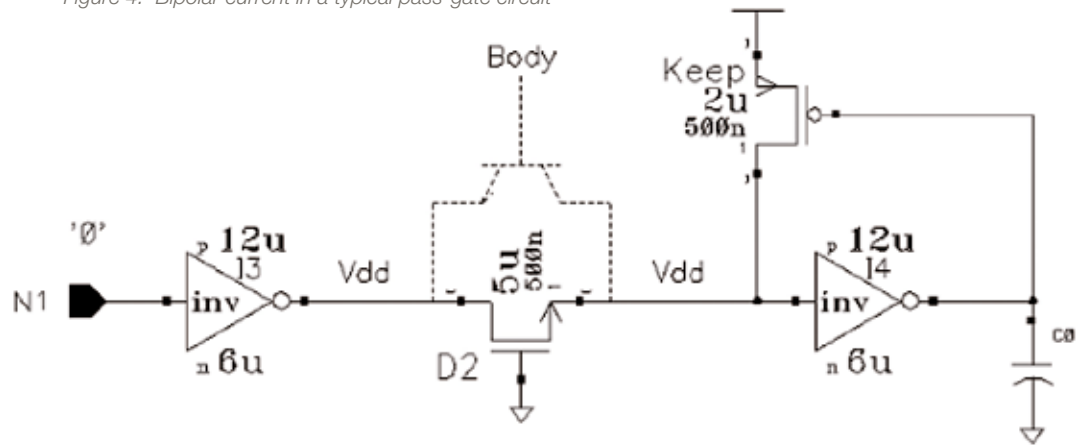
2. bipolar current

There is a low gain parasitic bipolar transistor on every floating body SOI FET transistors (Figure 3). This bipolar transistor is in parallel with the FET transistor and could cause false switching to the off FET transistor.

In general pass gate circuit has the highest bipolar current effect. This is due to the voltage of the drain and source of the pass gate transistor can be both at the supply rail (Figure 4). The collector and the emitter of the bipolar are at Vdd causing the bipolar base (body of the nfet) to charge up to Vdd as well. If the bipolar emitter is switching from Vdd to ground, there will be enough Vbe developed across the base-emitter junction to turn on the bipolar transistor. Even the nfet pass-gate is in its ‘off’ state, the switching inverter I3 could cause a false switch if there is enough bipolar current generated during N1 switches from a ‘0’ to a ‘1’. The designer needs to simulate this condition especially with a large selector design where there are many more bipolar transistors connected in parallel.

However over the years of the technology scaling, this bipolar current effect has been pretty much eliminated due to the reduction of the operating voltage of the 90nm node and beyond. In some extreme case, where the design has many transistors connected in parallel, the designer needs to verify the bipolar current to ensure the functionality of the circuit. This is particular important if the design will required functional burn-in at a much higher voltage than the typical operating voltage condition.

Figure 4. Bipolar current in a typical pass-gate circuit



3. local heating

The insulation layer of the SOI wafer creates a potential temperature delta between devices called local heating. Circuits with DC current, such as analog type of circuits, may have local heating effect. However this can be reduced or eliminated by using robust layout techniques for analog designs which are required for current density and electro migration issues. These requirements also help to spread the temperature of the analog circuits and minimize the temperature delta.

summary of SOI circuit designs

- ▶ Good design practices in bulk also apply to SOI
- ▶ There are additional circuit design issues in SOI that need to be considered
- ▶ Any bulk designs can be designed in SOI

1. floating body devices

- Use floating body as often as possible
- Greatest performance benefits from SOI
- Use model to understand floating body effects
- History effect is small but needs to be considered
- Bipolar effect is becoming less important

2. body contact devices

- Provides more control over DC operating point
- Use for matching transistor DC operating points
- Sense circuit for SRAM, analog circuits, etc.
- Less performance benefit
- Layout area penalty
- Reduces or eliminates history effect