Challenges and solutions for ESD protection in advanced logic and RF CMOS technologies

G. Groeseneken1, S. Thijs1, D. Linten, M. Scholz, J. Borremans2, N. Collaert, M. Jurczak
IMEC
Kapeldreef 75, B-3001 Leuven, Belgium
1Also at KU Leuven, ESAT Department, Leuven, Belgium
2Also with Vrije Universiteit Brussel

Bio Slide Presenter

Guido Groeseneken received the M.Sc. degree in electrical and mechanical engineering (1980) and the Ph.D degree in applied sciences (1986), both from the Katholieke Universiteit Leuven, Belgium.

In 1987 he joined the R&D Laboratory of IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium, where he is responsible for research in reliability physics for deep submicron CMOS technologies. From October 2005 until April 2007 he was also responsible for the IMEC Post CMOS Nanotechnology program within IMEC’s core partner research program. In 2001 he became also Professor at the KU Leuven, where he is responsible for the Erasmus Mundus Master in Nanoscience and Nanotechnology. In 2005 he became an IEEE Fellow and in 2007 an IMEC Fellow.

He has made contributions to the fields of non-volatile semiconductor memory devices and technology, reliability physics of VLSI-technology, electrical characterization of semiconductors hot carrier effects in MOSFET’s, time-dependent dielectric breakdown of oxides, Negative-Bias-Temperature Instability effects, ESD-protection and testing and plasma processing induced damage. Recently he also worked on characterization and reliability of high k gate dielectrics, FinFET and Ge-based MOSFET’s, integration of carbon nanotubes for interconnect applications and tunneling MOSFET nanowire devices.

He has served as a technical program committee member of several international scientific conferences, among which the IEEE International Electron Device Meeting (IEDM), the European Solid State Device Research Conference (ESSDERC), the International Reliability Physics Symposium (IRPS), the IEEE Semiconductor Interface Specialists Conference (SISC) and the EOS/ESD Symposium. From 2000 until 2002 he also acted as European Arrangements Chair of IEDM. In 2005 he was the General Chair of the Insulating Films on Semiconductor (INFOS) conference, organized in Leuven, Belgium.

He has authored or co-authored more than 300 publications in international scientific journals and in international conference proceedings, 6 book chapters and 10 patents in his fields of expertise.
Abstract

In this paper we review the challenges and possible solutions for the ESD protection of the new CMOS-based technologies. In the first part of the paper we will discuss the implications when classical scaling is maintained, and we will show that the ESD design window will be drastically decreased. Traditional ESD protection solutions, such as the dual-diode approach, will not be an option anymore and new techniques need to be introduced.

In the second part we review some of the recent results that have been obtained using Multiple gate technologies. We demonstrate that reasonable intrinsic ESD performance can be obtained, but achieving this desired ESD-robustness is found to be critically dependent on various design and process parameters. As a result the design of ESD protection for FinFET technology appears to be a challenging task for the future.

In the third part, we show that new solutions for the ESD protection of RF CMOS circuits can be obtained. These solutions can either be based on ESD-RF co-design solutions or in a ‘plug-and-play’ approach. As an example a novel T-diode protection approach will be demonstrated for the protection of an LNA for UWB-applications, achieving HBM protection upto 5 kV.

Outline

• Introduction

• Trends in technology scaling and impact on ESD

• ESD performance for MuGFET based technologies
  – Impact of layout
  – Impact of processing: SEG, silicide block, strain

• ESD problems and solutions for RF-CMOS applications
  – Co-design
  – Plug-n-Play

• Conclusions and outlook
Purpose

- To give an overview of the present trends in CMOS technology scaling
- To discuss the ESD robustness of future MugFET based CMOS technologies
- To show possible solutions for ESD protection of RF CMOS circuits

(Source: Intel)
Scaling made CMOS a feasible and competitive option for RF applications

RF CMOS compared to other RF technologies

Drive to low-cost high-volume applications
Scaling to sub-100 nm dimensions
⇒ CMOS is rapidly moving up to frequencies that were once the exclusive domain of the III-Vs.
The ‘Big Bang’ of microelectronics

- Tubes
- Semiconductors
- MOS
- CMOS

Magnetoelectronics
Polymer electronics
Optoelectronics
Nanoelectronics
Biosensors
M(N)EMS
Molecular nanotechnology

1950 1960 2000 2020

A Few (?) enabling R&D Breakthroughs

- MOSFET
- LOCOS
- Steppers
- KrF litho

Planar process
Ion implant
LDD
CMP

SIN Passivation
Plasma Etch
Silicide
Extensions / HALO
Cu metal

‘60 ‘70 ‘80 ‘90 ‘00

- Spike RTA
- ArF litho
- SION
- Channel strain
- Low-k dielectric
- Co-implant USJ
- Immersion litho
- High-K
- Metal Gate
- Multi-Gate
- SEG
- msec anneal
Technology options for continued CMOS scaling

Explosion of possible device technology options is a nightmare for reliability and ESD engineers
High-K/Metal gate hits production at 45nm!

Intel tips high-k, metal gates for 45-nm
(01/27/2007)
SAN JOSE, Calif. — Intel Corp. has disclosed more details about its 45-nm process, saying that it has implemented high-k dielectrics and metal gates for the technology.

“The implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s,” said Intel co-founder Gordon Moore, in a statement.

IBM shifts to high-k metal gates
Posted : 30 Jan 2007
Chip companies are joining the forefront for the use of high-k metal gates for chip transistors.

ESD problems and solutions?
• ESD implants SEG
• Silicide block
• Oxide breakdown?
• First results available
• Non-Si materials and devices?
• 32-22-16 Non-planar devices
• 45-32 Non-planar devices
• High-k, Metal Gate
• 90-65-45 Strain, USJ
• >=130 time
ESD Design window shrinks with technology!

Gap between oxide breakdown and holding voltage vanishes

ESD classical levels more difficult to achieve for each new technology node
**Impact of high k/metal gate on ESD performance**

![Graph showing gate stack robustness](image)

- Similar EOT (1.4 nm)
- No clear robustness improvement with high-k

**ESD Protection in RF applications**

- $C_{\text{parasitic}}$ of 600 fF @ 5 GHZ gives impedance of 53Ω!
- Series resistances of ESD protections lead to increase noise in the RF-circuits

**Comparison of ESD-RF trade-off**

<table>
<thead>
<tr>
<th>Device</th>
<th>Figure of Merit (A/pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ggnMOS</td>
<td>2.7</td>
</tr>
<tr>
<td>LVTSCR</td>
<td>5.4</td>
</tr>
<tr>
<td>Diode</td>
<td>12.5</td>
</tr>
</tbody>
</table>

**Table**

17

18
Basic ESD-protected common source amplifier

Worst case ESD path ESD stress RF\textsubscript{in}-V\textsubscript{SS}:

\[
V_{gs}(M_1) = (R_{ON,D2} + R_{VDD} + R_{ESD} + R_{ON,PC})I_{ESD} + V_{H,D2} + V_{H,PC}
\]

ESD design window Figure-of-Merit (FOM)
ESD design window: including power clamp (RC clamp)

No classical solution for 65 nm CMOS!

Impact of 2 kV HBM on digital circuit performance

At <100 fF, 2kV HBM can no longer be achieved
Is 2 kV HBM still Needed in the Field Today?

- ESD/EOS failures as provided by various members of the Industry Council
- Includes both automotive products and consumer ICs
- A vast majority of the returns are often found to be due to EOS
- Total return rate due to EOS/ESD fails < 1 dpm

No obvious correlation of EOS/ESD returns to HBM levels of 500 V … 2 kV

![Bar chart showing HBM robustness vs. EOS/ESD fails per million devices]

Supplier/Customer

“Cost of ESD”

Cost of ESD design
- dependent on
  - chip area
  - respins
  - resources
  - circuit performance
  - time-to-market

Technology node @ product qualification
- 90 nm 2003
- 65 nm 2005
- 45 nm 2008

2kV HBM Level
1kV HBM Level
Safe Handling Level

Courtesy C. Duvvury
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  – Plug-n-Play
• Conclusions and outlook

What’s next? The MugFET structure

• Narrow Si fin with gate wrapped around
• 3D device on SOI
• Recently also bulk MuGFET becomes attractive (lower cost !)
• Smallest feature is not $L_{gate}$ anymore but $W_{fin}$
• Family of devices (Pi gate, Omega gate, Tri-gate, …)
  ⇒ $\text{MuGFET}=\text{Multi-Gate FET (FinFET based)}$
Benefits of MuGFET devices

- Reduced short channel effects (multiple gate effect) ⇒ lower leakage
- Ideal subthreshold slope (better gate-to-channel coupling)
- Higher mobility (undoped channel)
- Reduced dopant fluctuations (undoped channel)
- Very close to conventional planar bulk processing

FINFET process flow

- FinFET follows conventional processing, it can be done in any Si pilot line.
- Process re-usability from conventional CMOS process is higher than 70%
- Additional restrictions:
  - FIN patterning: FIN CD control
  - Gate stack: conformality in HK and MG deposition
  - Junctions: conformality
- New process steps:
  - SEG for Rs reduction
  - Spacer defined FIN *)
  - Spacer *)
MuGFET’s are 3D-devices!

Design parameters:
- Gate length $L_G$
- Fin width $W_{\text{fin}}$
- Fin height $H_{\text{fin}}$
- Fin spacing $S$
- # Fins $N$

$N = \text{number of fins}$

SEM and XTEM
- 60 nm
- 20nm wide fin
- SEG
- TEM PICTURE
- smooth fin surface
- controlled buried oxide undercut and recess.
- good corner rounding
- conformal gate stack
- POLY-Si Gate
- 60 nm
- BOX
- Buried Oxide
- nitride spacer
- 20nm wide FIN
- Buried oxide
Strongly reduced silicon volume, 3D effects, new materials:

Is this the next nightmare for ESD protection?

Oh No! Is ESD Going to be MuGGed by Yet Another Technology Development??

Give me your ESD!

C. Russ et al, EOS/ESD Symp., 2005
MuGFET: Grounded Gate NMOS

First results were discouraging: unprecedented high ESD sensitivity → failure instantaneous after breakdown!

Device Characterization: Gated Diodes

Bulk diode
P+ P- N+

FinFET diode
P+ I N+

C. Russ et al, EOS/ESD Symp., 2005
H. Gossner et al, IEDM 2006
Device Characterization: Gated Diodes

- ESD decreases with factor 4 because of SOI!
- Intrinsic ESD performance FinFET better than SOI → ‘attributed to better cooling by 3D-fins’

![Graph showing current vs. voltage for different device types: Planar bulk, Planar SOI, FinFET SOI.]

gg-nMOS ESD area efficiency

\[ W_{\text{effSi}} = NW_{\text{fin}} \]
\[ W_{\text{total}} = NW_{\text{fin}} + (N-1)S \]

- \( W_{\text{fin}} = 30\text{nm} \)
- \( \text{Spacing } S = 145\text{nm} \)
- \( N = 40 \text{ and } 400 \)

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D. Trémouilles et al., EOS/ESD Symposium, 2007

It2 is 4-8mA/µm effective width, 0.5-1mA/µm total width
- increases with increasing gate length and drops again
- scales with number of fins
gg-nMOS ESD area efficiency

\[ W_{\text{effSi}} = NW_{\text{fin}} \]
\[ W_{\text{total}} = NW_{\text{fin}} + (N-1)S \]

It\(^2\) per effective width increases with decreasing fin width
Explanation: higher effective heat capacity of 3D-gate!

It\(^2\) per total fin width decreases with decreasing fin width
Explanation: more area overhead because of fin spacing

Impact of processing: SEG

Ron and It\(^2\) are strongly improved, holding voltage unaffected
Explanation: better heat removal and storage from drain/body junction due to larger fin dimension!
Impact of processing: silicidation

Silicide block improves $I_{t2}$ but at expense of high $R_s$ and maximum voltage!

D. Trémouilles et al., EOS/ESD Symposium, 2007

Silicide block is better only for wider fins!

D. Trémouilles et al., EOS/ESD Symposium, 2007
Slightly higher $I_{t2}$ is measured for n-MOS devices with strain, attributed to better current uniformity.

- Design methodology needed for minimum area solution
- Will be presented by S. Thijs et al at this workshop
Optimal ESD Device Design

% Area increase

- ESD target
  - 1kV HBM
  - $V_{MAX} = 3.5V$

See also presentation S. Thijs at this workshop!

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ESD protection methodologies

Plug-and-play

Co-design

IP libraries e.g. Low-C devices

RF-ESD co-design e.g. ESD devices in matching network

Plug and play ESD protection for RF

Goal:
RF performance
2 kV HBM ESD robustness
e.g. Dual-diode approach
Experimental results 90 nm : ESD

In+-V<sub>SS</sub> ESD stress

![Graph showing ESD stress vs time and voltage](image)

Failed at 550V, instead of >2 kV HBM

“Plug & Play” inductive ESD protection

- Inductor shunts ESD currents from the LNA core
- Added after the core LNA design ⇒ “Plug & Play”
- “Bidirectional” ESD device should not disturb the LNA performance
- 2kV reached in 90nm CMOS for 5 GHz

Thijs et al., ESD 2004
Additional local voltage clamping

$5kV\ HBM$ reached for $5GHz\ 90nm\ CMOS\ LNA$ by adding extra small diodes at gate to avoid overshoots.

Linten et al., VLSI Symp. 2005

Above IC-inductors

Use of low resistive high-Q above-IC inductors $>8\ kV\ HBM$ robustness but large extra area.

S. Thijs et al., ESD 2005
Transformer based ESD protection

- ESD inductor is placed underneath matching inductor → no area penalty!

ESD-RF co-design methodology

50 Ω environment @ f₀ @ NF @ Gain @ …

Integrate the ESD (and package) RLC parasitics in the RF functionality (signal path)
Matching blocks useful in ESD

\[ \pi \text{-type matching:} \]
- allows to independently set \( \omega_0, R_{S/L}, R_{S/L}^{\text{eff}}, Q \)
- acts as low pass filter (for off-chip ESD protection)
- very robust ESD circuit !!!

Co-designed ESD LNA circuit

5 GHz LNA in 90nm CMOS

150um wide
ggNMOS
12 \( \mu m^2 \) diodes
HBM – 1.9kV

Vassilev et al., ESD 2003
Janssen et al., CICC 2005
Wideband RF ESD protection?

\[ |Z_{ESD}| \]

\begin{align*}
\text{Wanted} \\
\uparrow \\
5 \text{ GHz} \\
\downarrow \\
f
\end{align*}

- Dual-diode
  - band width reduction
- Distributed-ESD
  - area penalty, series loss
- T-coil
  - Noisy, Integrated 50 Ohm resistance: not for RF LNAs
- Bootstrapping
  - Power dissipation during normal operation, area penalty: inductors in active amplifier

ESD for wideband RF LNAs

Kleveland, EDL 2000

Galal, ISSCC 2003

W Soldner, ISSCC 2007
T-diode solution

A “Plug-and-Play” ESD protection for wideband RF
  - preserves input matching of A

\[
S_{11,\text{ESDLNA}} = \left| S_{11,\text{LNA}} \right|
\]

D. Linten et al, ESD Symp., 2007

T-diodes act as artificial transmission line

\[
Y_{TL} = Y_T
\]

\[
C_s = \frac{\tau}{Z_c}
\]

\[
L = Z_c \tau \left( \frac{1}{4} + \frac{1}{\pi^2} \right)
\]

\[
M = Z_c \tau \left( \frac{1}{4} - \frac{1}{\pi^2} \right)
\]

\[
C_c = \frac{\tau}{Z_c \pi^2}
\]
Implementation in LNA

- 0.18 um CMOS 1p6m (thick top metal)
- Shunt-shunt feedback LNA
- $C_{\text{diode}} = 230 \text{ fF } (2 \times 65 \text{um width})$
- STI-diode triggered SCR as power clamp
- RF and ESD characterization

D. Linten et al, ESD Symp., 2007

Experimental results: ESD TLP

First results: weakest parts are T-diodes underpass
Improved architecture results

D. Linten et al, ESD Symp., 2007

Wideband LNA demonstrated with 5kV HBM protection
T-diode solution has potential upto 12 GHz!

<table>
<thead>
<tr>
<th>[kV]</th>
<th>+</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>IN</td>
</tr>
<tr>
<td>IN</td>
<td>6</td>
</tr>
<tr>
<td>VSS</td>
<td>4.6</td>
</tr>
<tr>
<td>VDD</td>
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Conclusions and outlook
Conclusions

- Explosively growing number of technology options poses tremendous challenges to ESD protection community!
- Shrinking ESD design window and cost/performance considerations are challenging ESD standardization bodies to relax HBM-specs!
- Despite initial discouraging results, MuGFET/FinFET devices show promising ESD performance, provided design methodology to select delicate layout optimum and adequate processing options are applied
- Recent years has shown tremendous progress in alternative solutions for RF CMOS applications, both narrow band as well as UWB, both plug-and-play as well as co-design solutions

Alternative substrates: Ge, III-V

Possible combination for 16 nm: new devices in the critical path combined with Si CMOS
- strained Ge pMOS: high hole mobility
- III-V (on Ge) nMOS: high electron mobility
More than Moore: heterogeneous integration of different technologies

MEMS and NEMS: see session F S. Sangameswaran et al.

Carbon based electronics: Carbon nanotubes and graphene nanoribbons

SWCNT vs MWCNT

SWCNT

$C = n_1a_1 + n_2a_2$

$n-m = 3i - \text{Metal}$

$n-m = 3i - \text{Semiconductor}$


Plastic/organic electronics

3D integration
Unexplored ESD problems are waiting for new solutions

ESD will remain a challenge for years to come!

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