

The PSP Model in RF CMOS Design

WHITE PAPER

Introduction

While the Penn State Philips (PSP) transistor model is rightly hailed as an excellent alternative to traditional BSIM models for RFIC design, RF designers need to be aware of how PSP models relate to actual device behavior. PSP models do require some judgment on the part of model developers. Equally important is an understanding of the way these models are used in an RF process design kit (PDK). Simply including PSP models in a PDK does not guarantee that designers get all of the advantages in simulation accuracy and efficiency promised by the improved modeling technique. Today's RF PDKs must support the models appropriately and also provide capabilities such as statistical evaluations and an effective inductance tool.

Because high-quality transistor models are crucial for predicting circuit performance and design margins — and thus minimizing silicon iterations — this white paper explains the technology behind PSP models and why their accuracy depends to some extent on how PDK developers implement the models. Additionally this paper shows how statistical evaluations can further help designers deal with the inherent variability of deep-submicron fabrication technologies.

These and other capabilities offer better RF simulation accuracy than ever before, despite the greater demands of advanced process technologies. RF designers can get this higher accuracy with less effort and therefore focus on improving circuit functionality while meeting tight constraints on power consumption and noise.

PSP Models vs. BSIM

PSP models belong to a new class of transistor models developed to solve the challenges of RF design. Specifically, RF transistors must operate across a wide range of bias conditions — from large signals in a power amplifier's saturation region to weak signals in a passive mixer's sub-threshold region. Additionally, RF transistor models must correctly represent signal characteristics such as harmonics and linearity.

As shown in this paper, PSP models meet these requirements by computing the surface potential in the gate region of a transistor's silicon/silicon-dioxide interface. Although the surface potential technique has been known since the 1960s, putting the necessary equations together comprehensively and implementing them into a compact model was achieved only recently by the Philips MOS Model 11 and Pennsylvania State University's SP Model. In 2005, these two models were merged and released as the PSP model, which was accepted for industry standardization by the Compact Model Council (CMC).

BSIM, the most widely-used transistor model in the industry, is based on DC measurements of current/voltage and capacitance/voltage relationships. Although good for quick simulations and sufficient for capturing DC bias conditions, BSIM does not adequately capture characteristics in a transistor's sub-threshold region and has other limitations for high-speed designs. By addressing these problems, the PSP transistor model is far more accurate for RF designs.

Overview of PSP Model Theory

Compared to other modeling methods, the surface potential approach underlying the PSP model uses an analysis that describes more closely the device physics of transistors. Hence, these models can accurately predict various physical phenomena, including Coulomb scattering, quantum-mechanical effects, noise sources, retrograde channel profiles and stress induced by shallow trench isolation (STI).

To see how the surface potential approach works, consider that a transistor's gate electrode is in contact with a region of silicon dioxide, which overlays the device's silicon surface (Figure 1). Changing the bias voltage at the gate of the transistor affects the potential at the surface of the silicon. This surface potential relationship can be formulated into an equation involving various process parameters, including the device's body factor and bulk carrier concentrations. This equation is a form of the Poisson equation and is known as the Surface Potential Equation (SPE), whose solution can be

obtained through its first integral. Obtaining the solution is not trivial, however, so the PSP model uses an approximation of the SPE based on the position dependence of the minority carrier effective Fermi level (imref). Equation (1) shows a generic form of the SPE [1].

$$\left(V_{gb} - V_{fb} - \psi_s\right)^2 = \gamma^2 \phi_t H(u) \quad \text{Eq. 1}$$

- V_{gb} : Gate-body applied voltage
- V_{fb} : Flat-band voltage (quantum mechanical concept, affected by presence of oxide charges)
- ψ_s : Surface potential
- γ : Body factor (dependent on process technology)
- ϕ_t : Thermal voltage
- $H(u)$: Square of the surface electric potential, where (actual function depends on the approximation of the minority carrier)

Understanding the terms of Eq. 1 in greater depth helps clarify how the surface potential model works. These parameters are all materials- and processes-dependent, and should therefore clearly reflect the physics of the transistor. With a voltage (V_{gb}) applied to the transistor's gate, beyond a certain threshold (V_{TH}) a conducting channel forms at the silicon surface and a current flows. The flat-band voltage (V_{fb}) is determined by the work function of the material stack in the manufacture of the transistor and any electrical charges in the silicon dioxide as a result of the manufacturing process. The surface potential to be determined (ψ_s) can be related to the parameters used in circuit analysis. The body factor (γ) is a function of silicon permittivity, concentration and oxide capacitance per unit channel area. The thermal voltage (ϕ_t), also known as the thermal potential, is determined by Boltzmann's constant, electron charge and temperature.

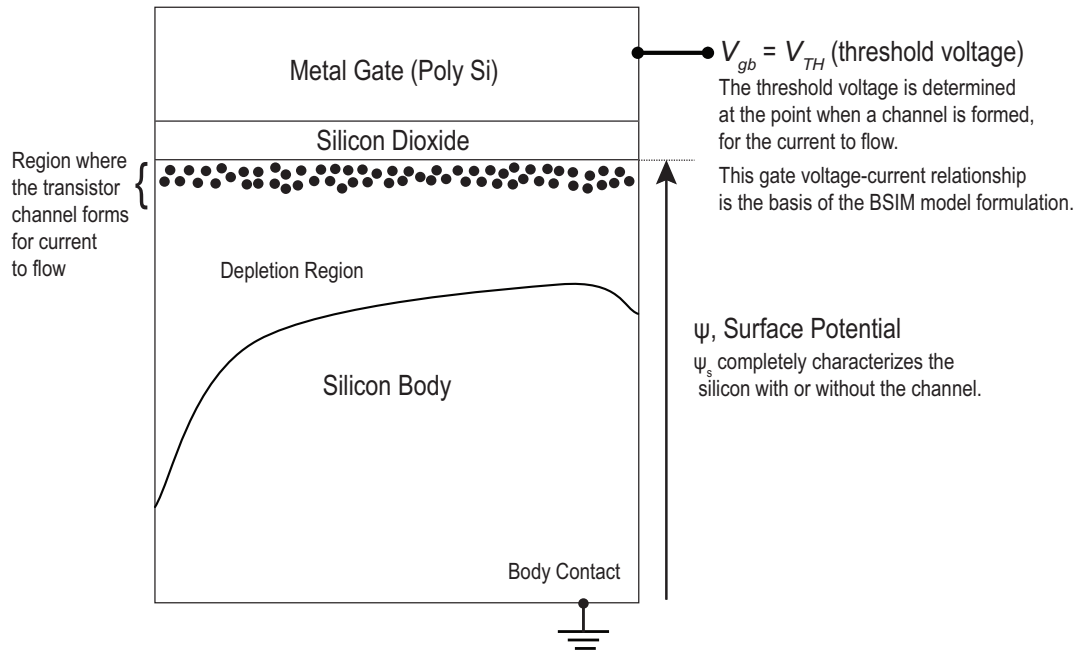


Figure 1 – Definition of the Surface Potential in the Voltage Equation.

Various works on surface potential models have suggested different definitions of $H(u)$. The PSP model uses an expression that considers the vertical dependence of the minority carrier imref. This approach implements a better-conditioned $H(u)$ that avoids simulator crashes associated with negative $H(u)$ values in previous models.

In addition to the PSP model, the generic form of the SPE is the basis for another popular surface potential MOSFET model — the HiSIM model — as well as the original Pao-Sah surface potential model [2]. The PSP model is, however, uniquely defined by the selection of $H(u)$ as a function that can be solved non-iteratively, thereby reducing simulation time. Consequently, a circuit simulator can efficiently compute the parameters needed for the evaluation of circuit designs, including the current flowing through the transistor, channel noise and other higher-order effects.

Implementing Practical PSP Models

In practical implementations, the surface potential model must be able to predict the currents for devices of different geometric sizes. Because this requirement can sometimes pose challenges for less-well-behaved transistors, PSP models can use geometric binning to improve accuracy. A model that implements geometric binning covers several bins in a single model. For example, bin 1 might span gate lengths from 0.09 μm to 0.15 μm , bin 2 from 0.15 μm to 0.5 μm , bin 3 from 0.5 μm to 1 μm , etc. If the circuit designer specifies the model with a 0.13 μm gate length, the model automatically selects the parameter values defined in bin 1 for simulations.

The binning method clearly emphasizes the correspondence of the model to measurement data from test structures, while weighing less on the ability of the model equations to represent device physics. No matter how good the model equations are at describing the physics of the transistors, random and systematic process variations sometimes cause variances in output currents or threshold voltages. Model

developers must decide how much emphasis to place on available process-variation data versus the output of the model equations that describe the device physics.

PSP models before version 103 (the latest version at the time of writing) required separate sets of parameters for defining a binning model type, a global model type (consisting of equations that describe the entire geometric range) and a local model type (which is not geometrically scalable). Subsequent PSP versions will unify the parameters into a single model type.

With this unification, any decision to switch from a global model to a binned model will be less costly in terms of model-development time. As a fabrication process matures and more variation data becomes available, model developers can clarify device characteristics better and capture any deviations with a binned model. Conversely, process data might prove that global models provide accurate results for certain devices. Either way, RF circuit designers get more accurate models.

Additionally, the latest PSP models still use fitting parameters because some equations governing the interactions contain parameters that cannot be obtained directly from measurements — contrary to common misunderstandings that these models rely exclusively on direct correspondence between the model and the underlying device physics. Thus, good model implementation depends on how the individual performing the extraction judges a good fit. In making such judgments, model developers must make tradeoffs such as obtaining a good fit for the drain current I_{ds} with scaling of the transistor width W or fitting margins for the output resistance R_{ds} within that scaling range. Changing one fit affects the other.

Thus, PSP models have not eliminated the need for careful work by experienced modeling engineers and scientists. These model developers must follow a clear methodology, or at least a set of priorities, for successful model extractions.

PSP Model Advantages

PSP models improve the accuracy of circuit analysis in several ways, including more accurate distortion simulation and better reproduction of device symmetry effects and higher-order derivatives. Large signal modeling or distortion is quite important in RF designs, and a good example can be seen in the representation of higher-order harmonics.

Specifically, a sinusoidal input signal to the gate of a MOSFET results in an output drain signal that contains the input frequency (fundamental) as well as higher-order harmonics. The MOSFET generates this distortion due to the non-linearity of the device's drain current and capacitance characteristics.

To model distortion effects well, it is important to model the higher-order derivatives of the drain current and capacitance accurately.

Figure 2 compares PSP and BSIM models for their reproduction of the first through fifth harmonic output power for an n-channel device [3]. (Similar results can be expected for a p-channel device since it shares the same model equations as an n-channel device in both PSP and BSIM.) The dashed lines in the figure show the actual results as determined by a more involved mathematical analysis [3].

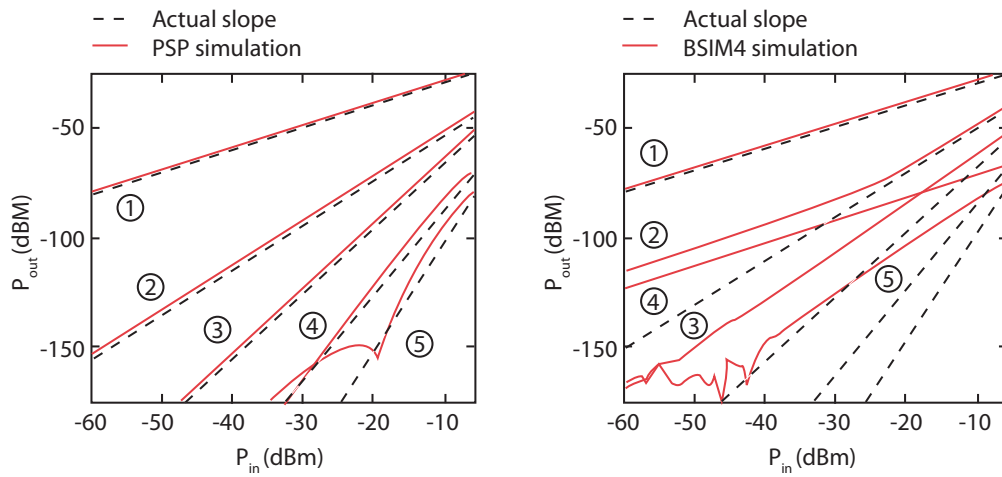


Figure 2 – First through Fifth Harmonic Output Power as a Function of Input Power Simulated with the PSP Model (left) and the BSIM Model (right) for an N-Channel MOSFET from 90 nm CMOS [3].

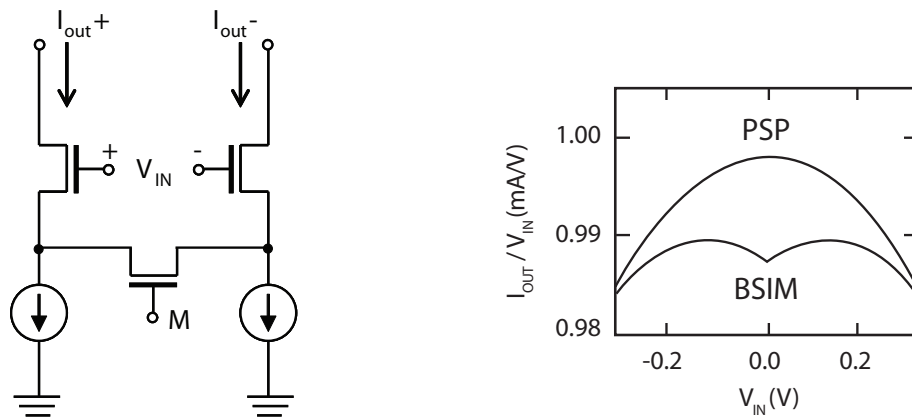


Figure 3 – Variable Transconductance (or V-I Converter) Circuit (left) and its Transfer Characteristic (right) Simulated with BSIM and PSP [3].

The dashed lines in Figure 2 correctly show that a higher gradient for the power curves of the higher-order harmonics. The BSIM model is not able to show this feature, however, and instead predicts a second-order harmonic in parallel with the fundamental. In contrast, the PSP simulations correctly reproduce the slopes of the first to fourth harmonics and show a fifth-order harmonic that follows the gradient of the correct slope at significant power levels. As these results indicate, replacing BSIM models with PSP models in RF circuit simulations can achieve much more accurate distortion results.

Another important factor in RF simulation is reproducing the effects of device symmetry and higher-order derivatives, since many circuits are biased symmetrically so that either a positive or negative drain-source voltage can be applied. The simulated derivatives must remain continuous and capacitances correctly predicted.

Figure 3 on the previous page shows a variable-transconductance circuit and its transfer characteristics simulated with PSP and BSIM models. The magnitude of the transfer is affected by transistor M's gate voltage, which is at zero DC drain-source bias. Transistor M also determines the shape of the transfer characteristics. In simulation using the BSIM model, a case of non-symmetry results in discontinuity of the characteristic curve at $V_{IN}=0V$ (when source and drain instantaneously interchange). As a result, the first derivative of the transfer curve (represented by the curve's gradient) is undefined at the dipping point. As noted in *The new CMC standard compact MOS model PSP: advantages for RF applications* [3], this problem causes "occasional simulator crashes."

The PSP model achieves better results by emulating the drain-source symmetry using good fundamentals. This model generates a continuous, smooth transfer curve that provides better accuracy as well as avoiding simulator blow ups.

The RF Process Design Kit

A process design kit (PDK) includes a collection of verified data files for use by a set of custom IC design tools. These files include schematic symbols, foundry-specific models, GDSII-layer technology files, parameterized cells (PCells), DRC/LVS runset, parasitic extraction runset and scripts that are run by the EDA tools to automate the generation and verification of design data. Figure 4 on the next page shows a generic RF design flow and how the PDK is expected to support it.

PDKs for RF design should continue to include BSIM models for legacy support. Some users express concern about simulation speed with surface potential models, although PSP models can actually run faster than BSIM because of the simple nature of PSP's physical equations and smaller number of parameters. In any event, providing BSIM models is still necessary despite their shortcomings, but adding PSP models to a user-focused PDK will greatly improve the confidence and efficiency of RF circuit designers.

A good PDK — More than PSP models

A good PDK is not a simple collection of generic models and tools. It provides a clear direction for the design flow as shown in Figure 4 on the next page, and PDK providers must substantiate this flow with enhanced support.

In particular, developers of PDKs for RF design must handle the PSP model appropriately to gain the greatest benefits for RF designers. For example, the core PSP model provides the most benefits for RF designs because it omits local and semi-global interconnection metals. But with the use of this model, simulations must now account for parasitics in the complete RF model consisting of the local and semi-global interconnection metals joining the transistor terminals to the circuit outside the transistor area. Even after precise identification by parasitic extraction tools, the parasitic impedances are difficult to correct because they are too

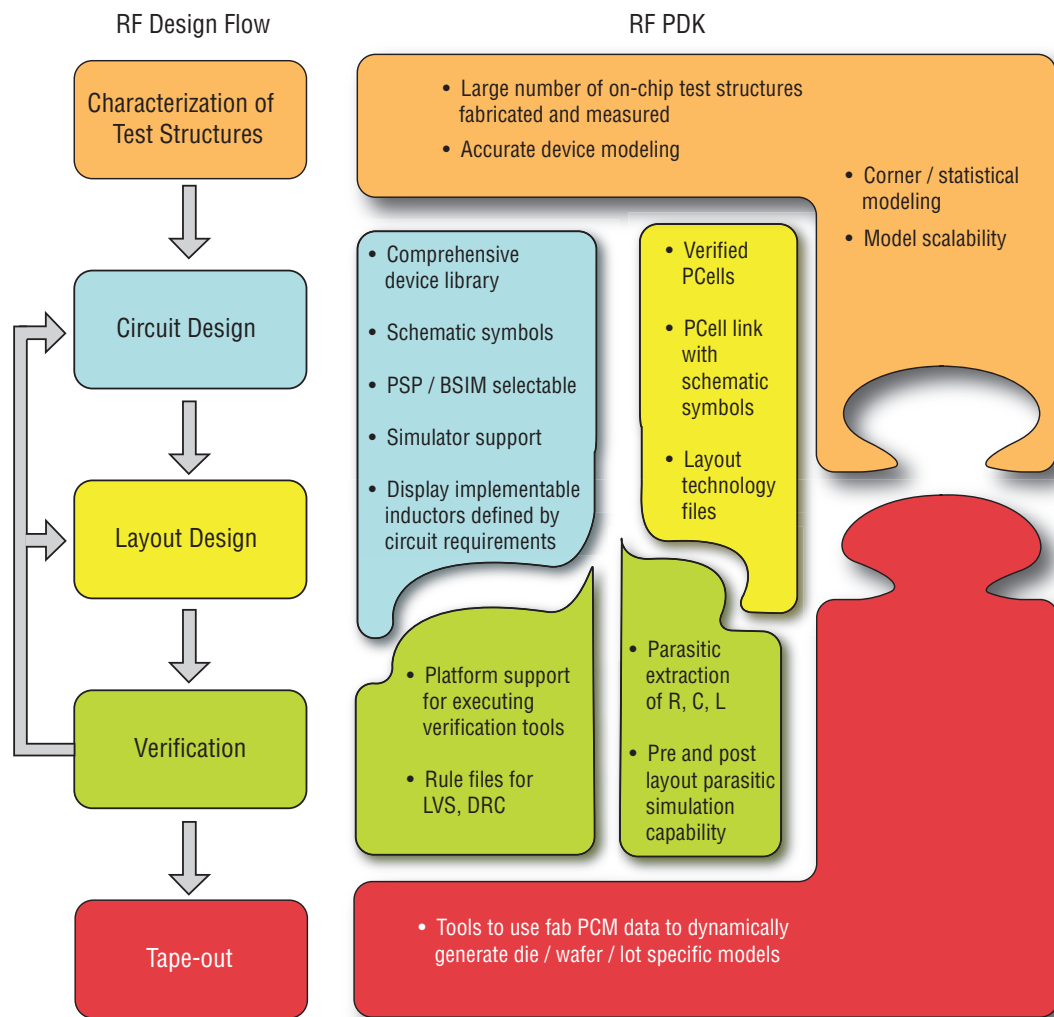


Figure 4 – The RF Process Design Kit (PDK) is Integrated to Support the Design Flow.

numerous in a large design. Yet the parasitic capacitances interact directly with transistors to change a circuit’s high-frequency behavior.

To deal with this issue, an effective PDK provides complete design blocks characterized up to the terminals where they are de-embedded. De-embedding removes the effects of the excess connection lines joining the device terminals to the points on the chip where they can be measured. This partitioning ensures that simulations consider only relevant effects starting from the terminals inwards to the design

block. The design block thus contains the core transistor and all interconnect metals leading to the outside of the block.

In characterizations such as these, model developers compare measured S-parameters to the outputs of models that include equations for parasitic descriptions. A good fit to high-frequency performance can be expected only if the model developers have correctly formulated these equations. Thus, poor preparation can defeat the excellent capabilities of the PSP model.

In addition to the tools outlined in Figure 4, an RF PDK must contain enhanced functionality for success with today's deep submicron CMOS technology:

- **Accurate PSP models with simulator support** — RF device models typically include MOSFETs, resistors, MIM/MOM capacitors, varactors and inductors. Accurate SPICE models have to be created from characterizations of test structures and also work in popular simulators such as Cadence Spectre and Agilent GoldenGate. For future RF designs moving towards millimeter-wave frequency bands, transmission-line models will also become necessary.
- **Statistical modeling capabilities** — PDKs for sub-100nm technologies now require statistical modeling tools and appropriate variance models to deal with the relatively larger variations in these processes. A statistical modeling tool should be able to generate statistical distributions using Monte-Carlos analysis, in addition to typical 3-sigma fast and slow corners. Since the corners of each process parameter may or may not be independent, the tool must handle these statistics independently for analysis. A tool that implements this approach can evaluate the likelihood of designs hitting process-corner extremes and thus accurately predict the probability of design success. With this insight, design managers can realistically decide whether more time should be used to “tighten” a design.
- **An effective inductance tool** — Although designers can get good results using the traditional approach to designing inductors (designing a layout, then iteratively adjusting it based on electromagnetic simulations), this approach takes a significant amount of time. An effective inductance tool can greatly reduce the necessary time and effort by generating inductor layouts based on the designer's electrical specifications. Additionally, accurate parasitic inductance extraction and adjustment can give designers the confidence to take a less conservative approach in the spacing of on-chip components, thus making more efficient use of the available silicon real estate.

Summary

When included in a well-developed PDK, the PSP model serves as a great tool for RF designers. The model's surface potential fundamentals enable it to predict performance beyond what is possible with the BSIM model. A complete PDK for today's RF designers thus adds PSP models to the existing package of BSIM models, other models and verified data files. This complete PDK integrates tightly with the RF design flow to allow RF designers to focus on circuit design issues rather than the accuracy and usage of the tools.

Additionally, a good RF PDK for deep sub-micron technology should provide effective statistical and inductance tools. These tools save time as well as giving designers the confidence to get the best performance and efficiency out of the silicon technology. With advanced models and tools, designers can meet tight constraints on power consumption and noise, while minimizing time to market and improving device manufacturability.

For more information on Fujitsu Manufacturing Services capabilities, please visit the company web site at <http://www.fujitsu.com/us/services/edevice/microelectronics/sms/> or send e-mail to inquiry.fma@fma.fujitsu.com.

References

- 1.G. Gildeenblat, Z. Zhu and C.C. McAndrew. *Surface potential equation for bulk MOSFET*. Solid-State Electronics 2009;53:11-13.
- 2.H.C. Pao and C.T. Sah. *Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors*. Solid State Electron 1966;9:927-37.
- 3.A.J. Scholten, G.D.J. Smit, B.A. De Vries, L.F. Tiemeijer, J.A. Croon, D.B.M. Klaassen, R. van Langevelde, X. Li, W. Wu, and G. Gildeenblat. *The new CMC standard compact MOS model PSP: advantages for RF applications*. RFIC Symposium 2008;247-250.

FUJITSU MICROELECTRONICS AMERICA, INC.

Corporate Headquarters
 1250 East Arques Avenue, M/S 333, Sunnyvale, California 94085-5401
 Tel: (800) 866-8608 Fax: (408) 737-5999
 E-mail: inquiry@fma.fujitsu.com Web Site: <http://us.fujitsu.com/micro>



©2009 Fujitsu Microelectronics America, Inc. All rights reserved.
 All company and product names are trademarks or registered trademarks of their respective owners.
 Printed in U.S.A. WFS-WP-21351-03/2009