Floating Body Cell for Embedded and Standalone DRAM

Pierre Fazan
Innovative Silicon (ISi)
1015 Lausanne, Switzerland
Outline

- Introduction: memory space & RAM scaling
- History: Capacitor-less DRAM, FB memories, Z-RAM® floating body memory
- Bit cell operation: FB memories & Z-RAM® floating body memory
- Bit cell structure
- Standalone memory applications (DRAM)
- Embedded memory applications (SRAM, eDRAM)
- Memory scaling & roadmap
- Future challenges
- Conclusion
Introduction
RAM Memories

- SRAM, eSRAM
- 6T, 8T bit cell
- Memory process or CMOS logic process
- 80 F$^2$ dense
- 150 - 200 F$^2$ High perf.

- DRAM, eDRAM
- 1T/1C bit cell
- Memory process + C or logic process + C
- 6-8 F$^2$ stand alone
- 20-50 F$^2$ embedded
SRAM Scaling

- SRAM, eSRAM bit cell scaling issues:
  - 6T, 150 F^2 area
  - Lower Vdd: reduced Static Noise Margin (SNM) & Write Margin
  - Tox limited scaling: less device variation scaling (σVt ~ Tox)
  - Vt scatter, Line Edge Roughness
    - Small L and W devices
    - Reliance on Vt matching
    - High Vt devices
  - Leakage control
  - SER issues
- SRAM, eSRAM bit cell is no longer able to scale linearly: 8T

Source: Freescale, 2006
DRAM Scaling

- DRAM bit cell scaling issues:
  - 1T/1C: was 8 F^2, now mostly 6 F^2, moving to 4 F^2
  - STacked Capacitor (STC), TRenched Capacitor (TRC) cells: capacitor scaling
  - High k materials integration
  - Capacitor & contact aspect ratio
  - Self Aligned Contact (SAC) etch
  - 3D access device Recessed Channel Access Transistor (RCAT)
eDRAM Scaling

- eDRAM bit cell scaling issues:
  - 1T/1C: increasing cell size factor: 20 $F^2$ to 50 $F^2$
  - 3-9 extra litho steps
  - Capacitor scaling
  - Thermal budget
  - 2x–3x denser than SRAM at same node

Source: various NEC & IBM publications
How to Simplify & Scale RAMs?

- Single memory cell concept: 1Transistor only bit cell: 1T vs 1T/1C or 6T or 8T
- 1T to store and sense a data state
- Use current for readout: gain cell
- The same device stores & amplifies the data for sensing
- Possible with any Floating Body device
- Initially demonstrated on SOI devices: Floating Body Memories (FBM)
- Also possible on bulk Si with some form of isolation
1T Concept, FBM

- Exploit isolated (SOI or other) transistors Floating Body (FB) effect
- FB is used as a storage node
- Presence of carriers (holes) in FB defines a 1\textsuperscript{st} memory state
- Removal of carriers (holes) by junction forward biasing defines a 2\textsuperscript{nd} memory state
- Vt difference, current sensing
- Under development by many (ISi, AMD, Intel, Hynix, Samsung, Toshiba, Fujitsu, ST Micro,...)

Ex: NMOS

| SiO\textsubscript{2} | Si Buried Oxide |
|---------------------|--|-----|
| “1” Gate SiO\textsubscript{2} + + + + Buried Oxide Si |

| SiO\textsubscript{2} | Si Buried Oxide |
|---------------------|--|-----|
| “0” Gate SiO\textsubscript{2} Buried Oxide Si |

IMEC, Oct. 16, 2009
History
History (31 years)

- 2009: Hynix/ISi stand alone 6F²
- 2008: Samsung stand alone 6F²
- 2007: ISi Bipolar mode: Z-RAM,
- 2006: Intel vertical DG
- 2005: ISi FinFET data, Renesas TTRAM, Samsung SGT
- 2004: Fujitsu FinFET simul., ST Bulk Si, Toshiba FD
- 2003: Fujitsu GIDL programming
- 2002: Toshiba PD SOI, ISi LP op., UC Berkeley DG

First attempts
- 1978: 1st FB Mem. Report, Fujitsu, SOS
- 1990: 1st SOI Report, IMEC, PD SOI
- 2001: 1st bit addressable demonstration, Innovative Silicon, PD SOI

Time

Activity Level

Memory Array design (bit address)
Bit Cell Operation
2001: FBM

- 2001: 1st bit addressable memory proposed by S. Okhonin et al. (Innovative Silicon), IEEE SOI Conf. Positive biases
- 2002: T. Ohsawa et al. (Toshiba), ISSCC Conf. Positive & Negative biases
- Both states obtained by pulsing 2 terminals: possibility to create bit addressable memory
- Write state “1” by MOS impact ionization
- Write state “0” by junction forward biasing
- 3 ns operation demonstrated by ISi
2007: Z-RAM® Floating Body Memory

- 2007: bipolar mode operation by S. Okhonin et al. (Innovative Silicon), IEDM Conf.
- BJT operation for write & read, hold in accumulation
- Key advantages: more margin, longer retention time, higher read current, lower power, less variability, more scalable (PD, FD, 3D)
- Named Z-RAM® floating body memory by Innovative Silicon
Z-RAM FBM SPICE Modeling

- Modeling of bipolar operation in Z-RAM floating body memory by accurately modeling:
  - MOSFET
  - Parasitic BJT
  - Impact Ionization
  - Leakage currents
- Predicts Self Sustained Operation (SSO), write, read, programming window
Bit Cell Structure
Z-RAM Floating Body Memory Bit Cell

- On SOI, 2D PD or FD devices: isolation by buried oxide

- On bulk Si, 2D devices: isolation by buried well (triple well process)

- On SOI or Bulk Si, 3D devices: isolation by S/D

Source: Samsung

Source: ST Micro
Z-RAM Floating Body Memory Bit Cell (SOI Planar)

Cell density
Design complexity

Stand alone: 4 F²
Embedded: 25 F²

8 F²
45 F²

6 F²
35 F²
Standalone Memory Applications
Applications: Stand Alone

- 2D PD devices on SOI
- Example: $6F^2$, 54 nm memory array
- Presented at Symp. VLSI Tech. 09 (Hynix & Innovative Silicon)
Retention

- Typical retention time for standalone applications

![Graph showing current vs. holding time for different components]

- Holding time:
  - Typical retention time for standalone applications
  - Current (µA/µm)
  - Retention
  - T = 85°C
  - >10 s
Device & Array Data

[Graphs showing device and array data, including plots of current density vs. voltage and failure rate vs. retention time with different parameters.]
Embedded Memory Applications
Applications: Embedded

- Design of Z-RAM floating body memory at 90, 65, 45 & 32 nm
- 2D PD devices on SOI
- 45 nm Performance characteristics:
  - >3X eSRAM density
  - 2 ns read latency
  - 4 ns write latency
  - 2 GHz cycle time
  - Redundancy & ECC
  - Median static retention time 200 ms @ 85°C
  - Green bit map for simple functionality tests
- Presented at ISSCC 09 (AMD & Innovative Silicon)
Retention

- Typical retention time for embedded applications

![Retention Graph]

- Current (µA/µm) vs Holding time

- T = 85°C

- 100 ms
S/D Asymmetry

- S/D asymmetry obtained by adding an implantation step
  - Reduces operating voltage
  - Improves static retention time
  - Improves array yield
Memory Scaling & Roadmap
Scaling below 50 nm

Planar Devices: SOI
- Gate
- Source Drain
- Buried oxide
- Back gate (substrate)

3D Devices: SOI, bulk Si
- FinFET
- SGT

Stressors
- High K, Metal Gates

Sources:
- Samsung
- IBM
- Oki
- UCL

IMEC, Oct. 16, 2009
Scaling Example

- 11 nm FinFET on SOI demonstration

![Diagram showing scaling example with FinFET on SOI and graphs illustrating normalized programming window and cell current retention.](image-url)
Z-RAM Floating Body Memory Roadmap

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<td>Z-RAM ½ Pitch (nm)</td>
<td>58</td>
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<td>45</td>
<td>40</td>
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Standalone Memory Application
- Planar SOI

Embedded Memory Application
- Planar Devices on SOI

Planar SOI → 3D Devices on Bulk Si
Future Challenges
Future Challenges

- **Scaling**
  - Move from planar to 3D device structures for standalone
  - Voltage scaling

- **Retention**
  - Static retention: different specs for embedded and standalone memories
  - Dynamic retention: disturbs

- **Reliability**
  - Related to voltage & voltage scaling
  - Cycling: For DRAM replacement, need > 1E15 cycles

- **Concept, architecture, design & process solutions to these challenges**
Conclusion
Conclusion

- SRAM, DRAM scaling challenges
- 1T memory: simple solution
- Since 2001: array compatibility demonstrated
- Innovative Silicon: FBM then Z-RAM floating body memory
- No new materials needed
- Applications: standalone & embedded memories
- Z-RAM floating body memory roadmap:
  - Standalone memories: from PD on SOI to 3D on bulk
  - Embedded memories: from PD on SOI to FD on SOI
- Z-RAM floating body memory future challenges: scaling, voltage, retention, reliability
- Z-RAM floating body memory: a better RAM

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