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Forecasted Impact of Fully Depleted SOI Technology on Design

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Abstract

As potential users of Fully Depleted Silicon-on-Insulator (FD-SOI) technology for the 22nm/20nm CMOS node and beyond realize its many interests, the question of its impact on design practices arises. Although FD-SOI for next generation technology nodes is not on commercial offer yet, it is nevertheless important to bring early answers or indications to that question. This document therefore proposes a synthesis of what is known or can be reasonably expected from FD-SOI from a design perspective, and indicates some interesting new potentialities that designers may be able to exploit.

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Introduction

Fully-Depleted Silicon On Insulator, FD-SOI, is emerging as a promising solution to continue the CMOS scaling roadmap at the 22nm technology node and beyond, especially for Low Power and System-on-Chip applications. Compelling simulation and silicon data for nanometer scale transistors is becoming available. However, as potential users realize the many interests of this technology, the next question is: what about design ? Would a transition to a Fully-Depleted SOI technology mean a lot of disruption at design level? With FD-SOI processes for the 22nm/20nm CMOS node still in demonstration phase, it is early to give complete answers; on the other hand, this is an important factor in the decision to fully engage in this technology, so it is worth sketching the best picture possible at this stage. This document therefore intends to synthesize what is known or can be most reasonably expected when designing for FD-SOI; it will also indicate some new potentialities opened up by FD-SOI that designers may be able exploit. It builds upon information released in publications such as those listed at the end of this document or workshops organized by the SOI Consortium.

It hopes to demonstrate that a transition to FD-SOI could be, to a large extent, a continuation of current design practices rather than a revolution, with some added benefits for designers.

After a quick overview of the FD-SOI technology and the opportunities it offers, this review will address its impact on design from System-on-Chip integration level, through complex IP level, down to foundation IP and library design level.

1. FD-SOI Technology Reminder

Fig.1-1 is a reminder of SOI transistor structures. Modern FD-SOI structures as envisaged for the 22/20nm node and beyond rely on a silicon layer as thin as 5 to 8 nm at fabricated device level (UTSOI, Ultra-Thin SOI) over a Buried Oxide (BOx). The BOx can be relatively 'thick' (for example 145nm, as commonly used in Partially Depleted SOI digital chips today) or ultra-thin i.e. in the 10-30nm range (UTBOX, Ultra-Thin Buried Oxide).

Optional usage of an ultra-thin BOx is typically for some or all of the following reasons:

- relaxing of silicon thinness requirement (thus limiting the need for continually thinner transistor body at future CMOS nodes like 16nm-11nm-8nm),
- better transistor characteristics for some parameters (notably those related to electrostatic control of the channel),
- ability to locally remove top silicon and BOx to reach the base silicon and co-integrate devices on SOI and devices on Bulk with a small step height between an SOI zone and a Bulk zone, compatible with lithography tools,
- ability to implant back-planes under the BOx, also to bias them. This may be used for shifting V_T (transistor threshold voltage) or for implementing low power design techniques extremely similar to body biasing in Bulk CMOS technologies (more on that in the chapter dedicated to Low Power techniques). *Fig. 1-2* illustrates the general concept of back-biasing at CMOS device level. The type of back-planes (n+/p+) depends on the objective pursued, and different "backplane type, bias voltage" couples may be envisaged for a similar effect *(Ref. [6-9])*.

On the other hand, using an ultra-thin BOx comes with a somewhat more complex process integration.

See also *references [1-5], [12-14], [16]* for general information on the FD-SOI technology.

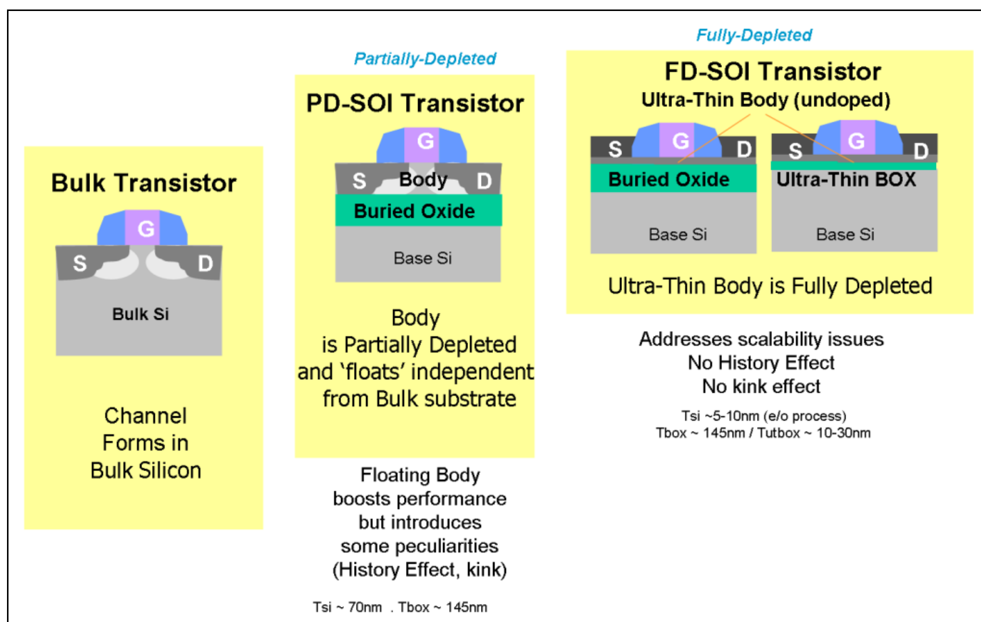

Fig.1-1.a. *Bulk and SOI Transistor Flavors*

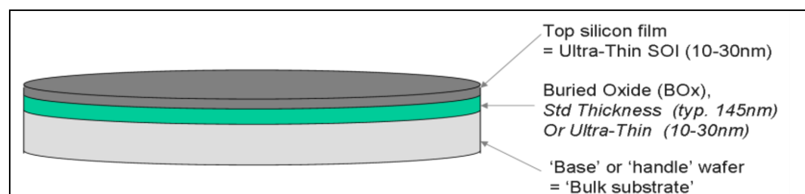

Fig.1-1.b. *SOI Starting Wafer for Fully Depleted CMOS Technology*

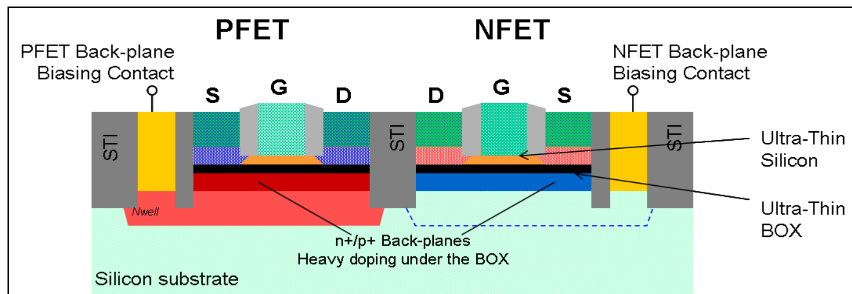

Fig.1-2. *Optional Back-biasing Concept (an application of Ultra-Thin BOx)*

2. Opportunities for Designers

Figure 2-1 shows how a few unique features of FD-SOI — namely the absence of channel doping, the ultra-thin body, the resulting excellent electrostatic control of the channel, plus the total substrate isolation — enable devices that can be used very advantageously from a design and product perspective for low power System on Chip.

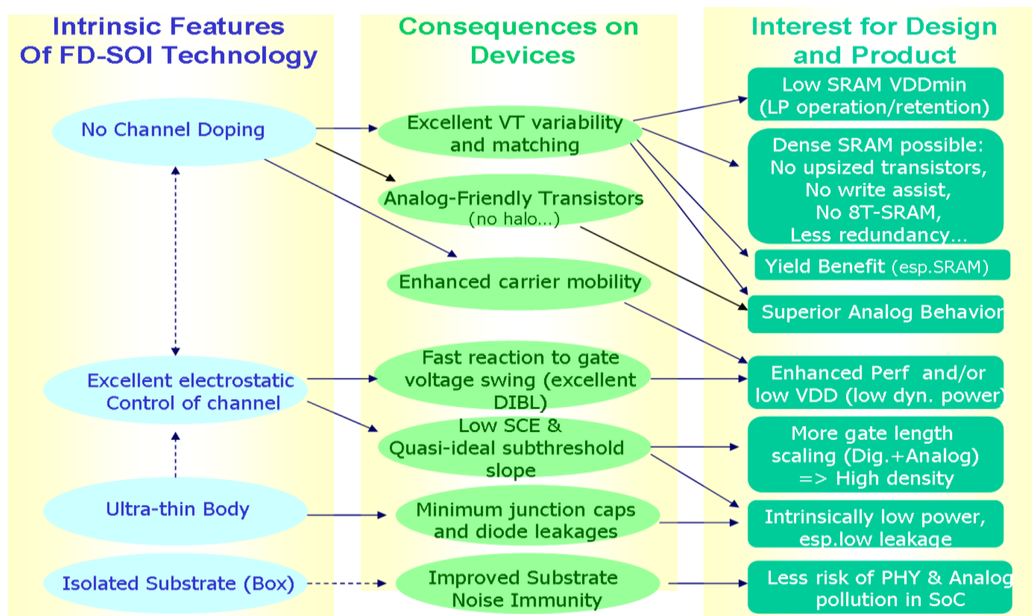

Fig.2-1. *Relating intrinsic features of FD-SOI technology to SoC advantages*

As can be inferred from the figure, interests for designers include the following:

SRAM VDDmin, area, yield

SRAM scaling (area and power supply) in traditional CMOS is becoming blocked by the variability issue : statistical V_T fluctuations in particular cause the actual Static Noise Margin, SNM, across an SRAM macro to degrade very much. For nanometer scale nodes such as 22nm, this means poor yield, impossibility to further scale V_{DD}, and/or counter-measures such as more embedded bit cell redundancy, departing from minimum size transistors, design tricks such as write assist, or usage of an 8-transistor bit cell – and all these counter-measures degrade SRAM density.

Conversely, FD-SOI, by offering a much improved V_T variability (plus good dynamic read and write currents), enables remarkably better results in terms of minimum V_{DD}, SRAM density, and yield *(Ref. [10], [11], [5], [2]).*

Further, some studies suggest that FD-SOI might bring renewed interest to 4T SRAM, taking advantage of the ability to reach very low leakage with high V_T FD-SOI devices and of the intrinsic V_T stability of FD-SOI (*Ref. [7]).*

Leakage

In terms of leakage, FD-SOI benefits from the very good Short Channel Effects and Sub-threshold Slope that come with the electrostatic control of the channel, low junction leakage intrinsic to the ultra-thin body over buried oxide, and from the ability to use retention modes at very low V_{DD}.

Digital Performance (Max frequency)

Digital performance is enhanced by the superior electrostatics of FD-SOI: better electrostatic integrity acts as a dynamic performance booster on transistors in CMOS logic structures – and the lower the power supply, the more pronounced this effect. Low junction capacitance also helps boost dynamic performance. In addition, the absence of channel doping enables better carrier mobility (due to less impurity scattering and lower effective vertical electric field) which in turn means better dynamic performance. A portion of this performance advantage may be offset to some extent by a higher source/drain access resistance (a specific challenge of ultra-thin film), however technologists are now proposing schemes to keep it at an adequate level *(Ref. [2], [8])*.

Besides, low variability of V_T means little dispersion of performance, which in turn leads (for a given nominal performance and in absence of compensation techniques) to a better guaranteed (i.e. sign-off) performance -- since the tail of V_T distribution will define worst-case performance of library elements, used for design sign-off in worst-case corner.

Dynamic Power Consumption

Dynamic Power Consumption directly benefits from the enhanced performance of FD-SOI, as it means it is possible to lower the operating voltage V_{DD} and still obtain remarkable performance (and dynamic power is proportional to V_{DD}^2). This is important for many low power applications, which, even though they may require high peak performance for some use cases, in typical usage are only rarely operated at peak performance (consider for example a smartphone being used to listen to MP3 audio). In addition, low junction capacitances of the ultra-thin body over a buried oxide, and ability to operate SRAMs at low V_{DD}, are added benefits in terms of dynamic power consumption.

Finally, from a broader perspective, FD-SOI with its excellent V_T stability enables a path towards operation at near or sub-threshold.

Digital IP Density

Two main factors are expected to enable FD-SOI at future nodes to continue area scaling according to Moore's law. One is the ability to design dense SRAMs with adequate yield, as noted earlier. The other is the ability to scale down transistor gate length (leaving more space for contacts and therefore facilitating reaching aggressive inter-device pitch) because FD-SOI enables regaining control of Short Channel Effects.

Analog behavior

The absence of channel doping and halo or pocket implants, the low level of Short Channel Effects and the excellent V_T matching that can be expected from an FD-SOI technology mean, at equivalent channel length, transistors with superior analog performance *(Ref. [2], [5], [12])*. Very good values for transconductance (g_m), drain resistance (r_o) and on-conductance (G_{on}) are expected *(Ref. [15-16])*.

Native Noise Isolation in SoC

One more potential advantage of SOI in the field of System-on-Chip, where Analog IPs or PHYs are co-integrated with a lot of digital logic, comes from the buried oxide. Analog IP are sensitive to noise that may propagate throughout the substrate, originating from neighboring IPs or even the IP itself. High Speed PHYs, which are physical layers of high speed digital interfaces (such as external DDR SDRAM, HDMI, etc.) carrying signals in the GHz range, are also very sensitive to switching noise from neighboring digital IPs.

The Buried Oxide layer may help shield Analog IPs and PHYs from such noise, resulting in better signal-to-noise ratio within the IP. It is expected that noise in a band up to a few hundred MHz should be reduced; however the magnitude of this effect will depend on the selected BOx thickness (thinner Box means more capacitive coupling). Many signals in a typical SoC do toggle in that frequency range.

Interestingly, analog IPs in a SoC are typically surrounded by a 'guard ring' for shielding them from substrate noise; therefore better native isolation may enable removal of that ring and saving some silicon area.

Analog/PHY IP Density

Analog IPs in modern SoCs have, proportionally to digital, stopped scaling for some time: their area remains roughly constant from one node to the next. Introducing FD-SOI at forthcoming nodes could be an opportunity to reintroduce some scaling there, with two levers : reducing the typical analog transistor dimensions and simplifying the overall circuitry. More specifically :

- Analog transistors typically employ long channels, to get decent conductance and process spread and keep clear from Short Channel Effects like steep V_T roll-off, and to guarantee a good gain. Therefore, if an analog designer has at hand analog transistors for which these effects are less pronounced, then he may use shorter channel lengths for the same quality of result and thereby design a denser block (with the added interest of faster operation if needed). In addition, a reduction of the channel length L can be accompanied by a reduction of channel width W to keep constant W/L ratio, typically when a given output current is required. Obviously other considerations such as sensitivity of small devices to noise etc. must be taken into account, but this is an area worth investigating.
- At circuit level, analog IPs or PHYs often include structures designed to compensate for variations in transistor characteristics – offset compensation is one example; there are many. Since FD-SOI technology significantly lowers the amount of inherent variability, then there are also potential area savings worth investigating in this direction.

3. Design Kit and Compact Modeling

3.1. Design Kit

For each new technology node, a Design Kit needs to be developed and provided by the Foundry. The Design Kit, or PDK (Process Design Kit) consists of the following elements:

- Design Manual (Layout Rules & Electrical Parameters)
- Layout Design Environment (Transistors and Layers Description)
- Layout Verification Runsets (DRC, LVS, Antenna etc.)
- Layout Extraction Runsets (Active and Passive)
- Device Compact Models

It is not expected that introduction of an FD-SOI based technology should significantly modify the amount and type of efforts that need to be deployed anyway to deliver the first 4 items in the above list (independently from the efforts required to set up a satisfactory FD-SOI process). Obviously some design rules and layout verifications will slightly evolve; for example antenna rules or anti-latch-up rules will be different and designers involved in such verifications should be aware of this, but the same applies when switching to any new technology node.

The Design Kit itself is exploited through CAD tools. PDK information is described through files that CAD tools understand. Overall, again, it is not expected that FD-SOI should require efforts to adapt CAD tools that would be significantly different from those required at any new CMOS node. It is required, however, to integrate Compact (aka SPICE) Models fit for FD-SOI on ultra-thin silicon film; this aspect is discussed below.

3.2. Compact Models

Two approaches are proposed today for obtaining a compact model fit for simulation of undoped Ultra-Thin Body Transistors with optional back-bias.

- One is to enhance existing SOI compact models to handle such FD-SOI devices. This is what the latest BSIMSOI model (BSIMSOI 4.x) from UC Berkeley proposes. In that case, the ecosystem already exists, creation and calibration of SPICE model cards follows the same flow as what is classically done for Bulk or PD-SOI *(Fig. 3-1.a.).*

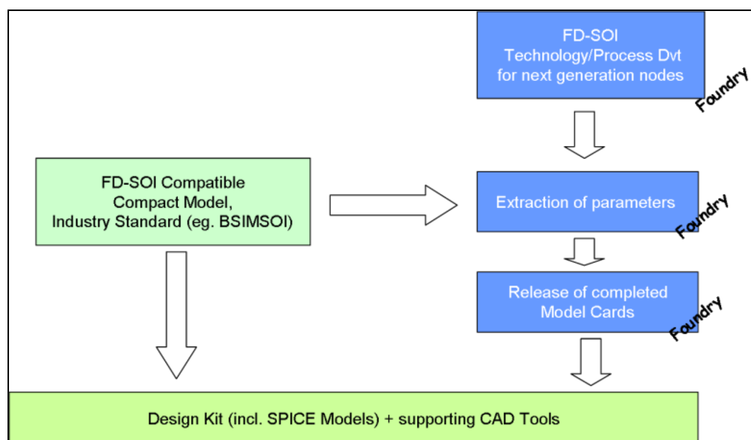

Fig.3-1.a. Release of SPICE data for FD-SOI based on industry standard model

- An alternative solution is to develop a model specific to Fully Depleted Ultra-Thin Body Transistors, considering that the physics that govern these devices is different from that of Bulk or PD-SOI devices (for example, there is no heavy channel doping, and electrostatics is fundamentally different). R&D Centers that have worked on such modeling include LETI, UC Berkeley and the University of Florida. This kind of model is closer to the actual physics of the transistor, and some of its proponents argue it provides more reliable extrapolated results when departing from the conditions at which the model has been calibrated, and therefore is more trustable to build predictive models. In that case, it is necessary to integrate such a novel compact model into commercial simulators and update extraction software so that it supports this new model: refer to *Fig. 3-1.b.* :
    - To be exploitable by simulators, the model may either be coded in Verilog-A, mostly independently from the target simulator, or may be incorporated into the C code of the simulator itself which requires intimacy with simulator code. The first solution is more modular and enables fast integration, the second solution is more intrusive into the simulator and typically requires collaboration with the EDA vendor but enables faster simulation and therefore analysis of more complex circuits (usage of Verilog-A could be a first step, native integration of "C" version into the commercial simulator could be a second step once FD-SOI technology takes off). The model is driven by parameters that provide all needed characteristics of the device as it is fabricated (geometry, physical parameters etc.); this parameter set is recorded into a SPICE "Model Card" (or its Verilog-A equivalent). Parameters that go into the Model Card are derived from measurements on silicon test structures (for example Id vs. Vgs curves, etc.). This extraction is normally done using some specialized tool that couples to the SPICE simulator and to the silicon under test and looks for best parameter values that will make the SPICE model fit the measured curves. In the case of usage of a novel model, the Model Card contains parameters that are specific to FD Ultra-Thin Body devices; therefore the extraction software must be updated to cope with this new model. This may require involvement or support from the vendor of the extraction software; however some extraction software packages enable users to customize extraction routines. At early investigation or development stage, it is also possible to extract parameters from TCAD (transistor physical structure level) simulations rather than from actual silicon devices. In addition, "predictive" or "silicon influenced models" may be developed by directly injecting target specifications, or by measuring electrical parameters under a restricted number of conditions and relying on the extrapolation capabilities of the model.

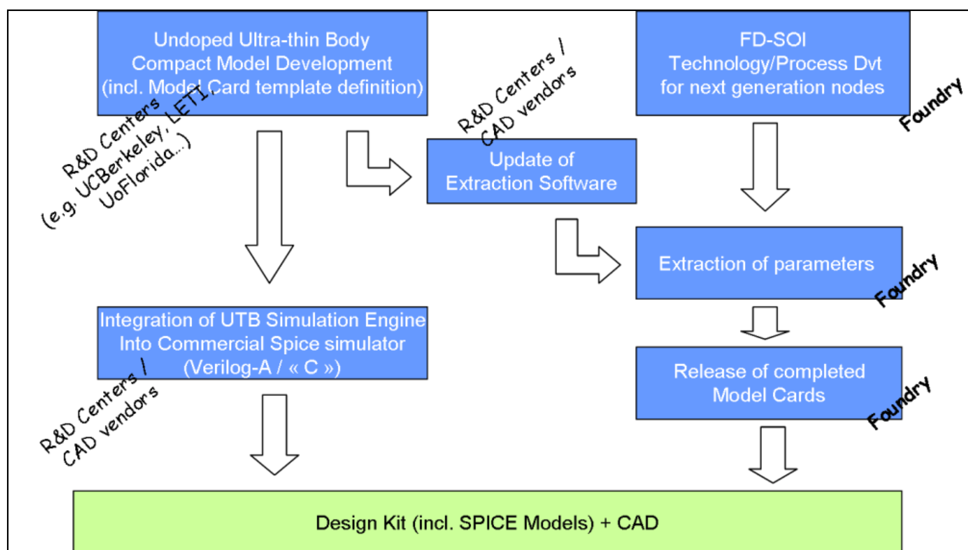

Fig.3-1.b. Obtaining SPICE Models optimized for Ultra-Thin Body Undoped FD-SOI physics

Overall: Compact Modeling of FD-SOI devices should not be a hurdle for introduction of the technology.

The fundamental work of understanding the physics and modeling the behavior of FD-SOI on Ultra-thin SOI (with optional Back-Bias) has been done. BSIMSOI4.x is an industrial solution publicly available today, and next generation models (e.g. surface potential based with specific care for modern FD-SOI devices) have been developed to a large extent even though they are not industrialized yet.

With FD-SOI Compact Models and a SPICE simulator capable of simulating them, the Designer can work as usual. He will create his circuit net list where each instantiated device calls its Model Card and will then simulate it using his SPICE simulator.

4. Design Flows – From SoC Level to Elementary Library Cell Level

Prior to going through the various aspects of Design, it is worth mentioning – as this affects many steps of the design flow – that FD-SOI is free of the Floating Body effect typical of Partially Depleted SOI. As a result, digital logic does not exhibit any history effect and analog circuits do not exhibit any kink effect or low frequency noise.

4.1. SoC Integration Flow

Fig. 4-1 outlines a typical System-on-Chip (SoC) Design Flow, from availability of a Design Kit to SoC Tape Out. It shows that System-on-Chip integration consists of putting onto a single die:

A. some complex IPs:

- fully synthesized digital functions (for example, a Video Decoder, a Graphics Engine, an on-chip Interconnect Bus, etc.),
    - these are based on libraries of pre-characterized standard cells and memories (SRAM, ROM)
- custom designed functions, imported as 'hard blocks' into the SoC layout,
    - analog blocks – like Frequency Synthesizer, Digital-to-Analog Converters etc.
    - Mixed Signal blocks or 'PHYs' (physical layer of very high speed digital interface, requiring specific design precautions) – like DDR, USB, HDMI or PCIe transmit/receive circuitry
- 'hardened' or 'manually optimized' digital blocks (for example, an embedded high performance CPU core), imported as hard blocks into the SoC layout
    - typically based on standard cells with manual optimizations especially at place and route level,
    - possibly with a little custom logic,
    - can be viewed as intermediate between synthesized digital functions and custom IPs,

B. I/Os, including ESD protections

C. Specialty low level IPs

- For example eFuse or Anti-Fuse, embedded Non Volatile Memory, etc.

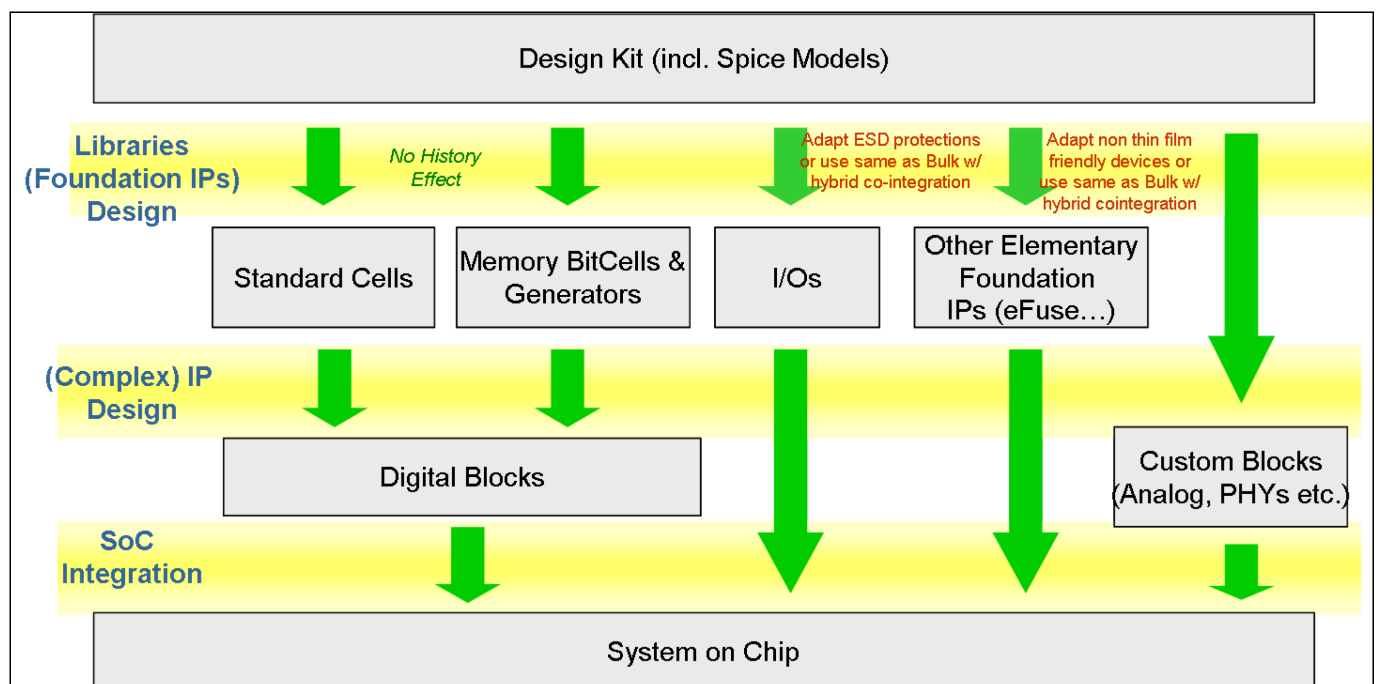

Fig.4-1. *From Design Kit to System-on-Chip*

Integration encompasses possible fusion of functional blocks into larger functional subsystems, functional verifications, physical synthesis, place and route itself, timing closure, layout and physical design rule checks. The fact that underlying devices are built on FD-SOI rather than Bulk is not expected to have any impact on those tasks. Integration flow is the same. In particular no specific sign-off corners and no additional libraries are expected to be required. Contrary to the PD-SOI sign-off flow, there is no need for min-max libraries to account for History Effect induced variability, and signal integrity and noise analysis will not need to be hardened to take into account any impact of history effect.

4.2. Complex IP Design Flow

4.2.1. Digital Block Synthesis Flow

Digital blocks in an ASIC are normally synthesized from a description of the function to accomplish in some high level language like VHDL or Verilog, or even "C". The synthesis tool picks standard cells and memory macros from libraries selected by the designer, trying to fulfill some performance and physical constraints indicated by the designer. In some rare occurrences, the designer might directly instantiate specific cells picked from such libraries.

In this flow, again, the fact that the standard cells and memory macros are made of transistors that will physically sit on an FD-SOI substrate does not change anything to the design flow. In other words, *usage of FD-SOI is fully transparent to digital designers*.

Standard cells and memory generators will be used in exactly the same way be they based on Bulk or FD-SOI transistors. The same list of parameters (propagation delays aka timing arcs, max load, footprint etc.) will be embedded in the library model describing a Bulk and the equivalent FD-SOI standard cell; the same thing applies to memories. Standard cells and memories will be used in exactly the same way along the digital design flow. In others words, from an SoC designer perspective, synthesizing and integrating a functional block onto FD-SOI rather than Bulk simply amounts to pointing to a different set of libraries; the design flow is unchanged. In particular, there is no need to analyze new, specific design corners.

4.2.2. Custom Design of Complex IP

4.2.2.1. Analog IP Design

From a design flow perspective, designing analog blocks using FD-SOI transistors is expected to be extremely similar to designing on Bulk:

- SPICE models can be used for simulation of FD-SOI analog blocks like they are used for Bulk Analog simulations.
- The absence of the Floating Body Effect in FD-SOI means no kink effect or other peculiarity has to be taken into account when designing and simulating FD-SOI Analog blocks.
- One slight difference for design (layout) is that FD-SOI transistors don't require substrate/well contacts (which makes FD-SOI analog transistor layout somewhat simpler), unless the flavor of FD-SOI technology used makes use of back-plane biasing. In the latter case, contacts to back-plane are required and would be inserted in much the same way as contacts to substrate/well in Bulk, only in the case of FD-SOI the contacts run through the BOx to reach the substrate (back-plane).

4.2.2.2. High Speed PHY Design

High Speed PHYs are physical layers of high speed digital interfaces. Although they carry digital signals, their high speed and/or sensitivity to noise are such that they require custom, analog-like design. Examples include logic that handles physical signals that run over interfaces to external DDR memory, PCIe/USB/SATA busses, HDMI cable, etc.

In some cases design will be at the transistor level, in some others it may rely on hand-instantiated standard cells with careful placement and layout. Electrical, analog-like simulation of SPICE models will typically be used.

Here again, as long as SPICE models and simulators for FD-SOI technology are available, usage of FD-SOI rather than Bulk based technology is expected to be transparent to designers.

4.3. Design of 'hardened' or 'manually optimized' complex IPs

Such blocks are mostly based on library cells, optionally with a little custom logic, and typically require carefully crafted place and route. They can be regarded as an intermediate approach between fully synthesized digital

blocks and custom block, addressed in the former paragraphs. Therefore usage of FD-SOI is not expected to introduce specific design flow issues for design of such blocks either.

4.4. Design of Libraries / Low level 'Foundation IP'

4.4.1. Standard Cells

Standard cells can be designed in much the same way as in Bulk. Simulation relies on availability of proper SPICE models. Complete optimization of the cells would take advantage of details of FD-SOI transistor behavior at target node, like fully optimized libraries on Bulk CMOS adapt to specificities of each new node. Such optimizations could possibly include, for example, taking into account different balance of capacitances, different optimal number of stacked transistor, etc. However, direct porting of a Bulk library to FD-SOI keeping the exact same cell micro-architecture (and in some cases the same layout) is an option even though the result may be sub-optimal.

Because FD-SOI is free of the 'History Effect', no specific characterization (like 1st switch/2nd switch transition times) to take it into account will be required vs. Bulk.

If the selected flavor of FD-SOI includes back-biasing, then it is necessary to contact the back planes. The PMOS half of the standard cell and the NMOS half of the standard cell may use a different type of back-plane (N or P) and biasing, much like one half is fabricated in N-well and the other half in P-well in traditional Bulk CMOS *(Ref.[7],[9]).* Some preliminary work is required before the actual design of libraries, with the objective to define a strategy on:

- what type of back-plane (n+, p+, or possibly none) and what biasing to use if the objective is to do multi- V_T,
- how to contact the back-planes (contact embedded in each standard cell, usage of filler cells, etc.),
- how to efficiently co-integrate different back-planes and layout the cells, eliminate risks of excessive inter back-plane leakage and limit process complexity (for example, avoiding triple well isolation).

Trade-offs may be a little different depending on whether the objective of back-biasing is Multi-V_T, or offering an equivalent to Adaptive Body Biasing used in Bulk, or both (also refer to next chapter on low power design techniques). It is expected that a foundry or IDM proposing an ultra-thin BOx with back-plane FD-SOI solution would provide guidelines to standard cell designers, especially regarding the backplane and biasing to use to obtain a given V_T with such a scheme (based on research like *Ref [9]*). Once the overall back-bias implementation strategy has been defined, contacts can be inserted in the same way as substrate and well contacts in bulk CMOS standard cells, with the difference that contacts now go through the BOx to reach the substrate (back-plane) in the case of FD-SOI. Contacts can for example be aligned on power rails in the standard cell, or embedded into dedicated "filler cells", as classically done on Bulk. The slight penalty area that may result vs. back-bias free FD-SOI depends on isolation between P-type and N-type ground planes: it is not greater than what isolation of P and N wells requires in classical Bulk. Adaptation of tools by CAD vendors is not expected to be a significant challenge, as handling of such Back-Planes is not very different from handling wells found in classical Bulk technologies.

4.4.2. Embedded Memories: SRAMs and ROMs

Embedded memories, like standard cells, can be designed with the same flow as on Bulk. If the selected technology is FD-SOI with a back-biased ground plane, then it is necessary to contact the back plane to apply the biasing voltage. Again, a strategy similar to that of classical Bulk may be used, with straps of contacts every so many microns, to reach the back-plane through the BOx and locally bias it *(Ref.[9]).*

In Chapter 2 "Opportunities for Designers", it was noted that SRAM are IPs to which FD-SOI brings very strong advantages : on top of that, in terms of design practices and design efforts, using FD-SOI will also lead to some relief as less SRAM design tricks will be required.

4.4.3. I/Os

The design of I/Os on SOI presents some specificities because of the presence of the BOx:

- ESD protections must be adapted,
- latch-up is not a concern due to complete isolation inherent to SOI,
- the rest of the I/O circuit should not need design techniques significantly different from Bulk.

ESD protections in Bulk CMOS usually include large diodes that reach into the substrate. With SOI, the substrate is isolated by the BOx and alternative solutions must be used. SOI technology has classically solved this problem by implementing ESD diodes as P-N junctions of devices fabricated in the top silicon. However the extreme thinness of the SOI film envisaged for 22nm technology node and beyond introduces new challenges, like lower breakdown currents. Research into the best ESD structures natively compatible with Ultra-Thin SOI is ongoing, however two alternative solutions exist today:

- during the CMOS process, etch off top silicon and BOx to build ESD protections into the base substrate, reusing structures used in Bulk CMOS; in that case usage of Ultra-Thin BOx helps reduce the height of the step between the Bulk zones (ESD protections) and the FD-SOI zones, to make it compatible with lithography tools.

- or, locally grow more silicon over the thin film to obtain a locally thicker film on which PD-SOI like ESD structures can be reused.

4.4.4. Other Low Level IPs / Foundation IPs

Design of other low level IPs is again not expected to be an issue as long as elementary devices and associated models are available. The work required here is more for technologists, to make available some specific devices on very thin silicon film and buried oxide. This aspect is addressed in the Appendix: "Device Availability".

4.5. Self-Heating

One concern sometimes expressed about SOI is self-heating: the presence of buried oxide could make the temperature of the channel rise more than in a classical transistor on Bulk, especially in the case of continuous current flow (e.g. in analog biasing circuits).

However, examining practices of designers that do have SOI experience, it appears that, as far as low power design is concerned, this is more a fear than an actual threat. They do not modify their design practices for self-heating concern. Simply, if wished (option turned on), SPICE models can model this effect and take it into account to make sure the simulations used to validate the design accurately represent the silicon's behavior.

Reasons invoked to explain why self-heating is not a practical threat include:

- Channel self-heating also exists in Bulk – the BOx would increase it to some extent,
- The time constant associated to local temperature rise is such that its effect is not a concern for switching logic,
- A significant proportion of the heat generated (both in Bulk and SOI) would be conducted by metal connections to the top side of the chip and package (therefore efficiency also depends on the packaging scheme, transistor dimensions etc.); and BOx has no impact on this mechanism,
- At a more global scale (block or die-level), the lower thermal conductivity of the SiO_2 BOx beneath the channel (lower than Si by 2 orders of magnitude) must be put in perspective with the ratio of BOx thickness (typically, 10nm for Ultra-Thin to 145nm for "thick" BOx) to finished wafer thickness (several tens of microns): thermal insulation of the BOx is relatively small (case of 'thick' BOx) to negligible (case of UTBOX) compared to the thermal insulation due to the Si substrate itself. In other words, evacuation of heat towards the bottom side of a finished wafer is not so much easier without a BOx than with a BOx. This rationale may be a little simplistic as interface and other nanostructure effects must be taken into account in a more rigorous analysis, but is an interesting first order.

4.6. Hybrid FD-SOI / Bulk co-integration

An intermediate approach that may be envisaged, possibly as an intermediate step in FD-SOI introduction, is a hybrid technology where all digital logic and memories and "safe" IPs exploit the benefits of FD-SOI, but a few IPs stay on Bulk: for example, some analog or specific IPs that designers prefer to keep on Bulk for any reason (legacy, etc.) – assuming the power/performance/variability crisis faced at the next nodes is not too acute for such IPs. *Figure 4-2* is a notional layout of a hybrid FD-SOI / Bulk chip; orange areas correspond to IPs kept on Bulk in this particular example. Finer granularity is also an option, where only a few very specific devices inside an IP would be on Bulk (for example, ESD protections of I/Os).

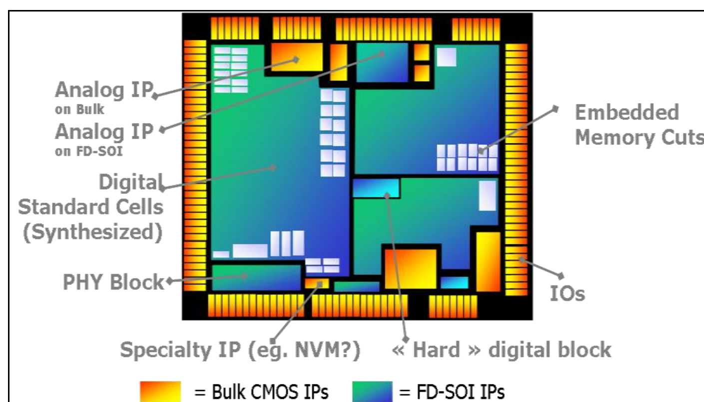

Fig.4-2. *Example layout of a hybrid FD-SOI / Bulk chip (notional)*

Some design rules may be associated to hybrid FD-SOI/Bulk co-integration (one could think, for example, of a minimum spacing between a device on Bulk and a device on SOI, to account for a transition zone): these should be taken into account in the PDK like all other design rules.

5. Low power Design techniques

Today, virtually all designs incorporate a certain amount of low power design techniques. Beyond the intrinsic behavior of the transistors available, these techniques enable the designers to further save active and leakage power by clever implementation. Some are introduced at a low level (for example, embedded in the automated synthesis design flow, like clock gating, or even at device fabrication level like CD biasing), others at the final application level (for example, Voltage and Frequency Scaling can be controlled per application by the Operating System).

The extent to which they are used and their sophistication depend on the target application.

Techniques used include:

- Dynamic Clock Gating,
- Micro-architectural RTL optimizations,
- Multi- V_T libraries,
- Static and Dynamic Power Switching,
- Retention Modes,
- Adaptive Voltage Scaling (AVS),
- Dynamic Voltage and Frequency Scaling (DVFS),
- Static and Adaptive Body Bias,
- Critical Dimension (CD) Biasing or Gate Length Biasing,
- Split Supplies.

With FD-SOI:

Most low power design techniques employed in traditional Bulk CMOS can be applied in exactly the same way in FD-SOI. Further, some of them will enjoy a magnification effect with FD-SOI: for example, AVS and DVFS will benefit from the ability to further lower V_{DD} for a given operating frequency; also, retention modes will benefit from the ability to set a low retention voltage on SRAM and have minimum SRAM leakage; etc. Multi-V_T and Body Biasing need to be transposed for FD-SOI (see below).

In addition, FD-SOI could offer opportunities to simplify some of those design techniques, depending on target applications. For example, in some cases the need for different voltage levels for RAM supply and standard cell supply may not be so justified if both SRAMs and standard cells can now be operated at the same low voltage (considering that FD-SOI significantly improves SRAM stability and VDDmin). Other opportunities might be worth considering, especially when a design technique is fairly complex for a second order impact.

Body Biasing:

Body Biasing, which can not be implemented in exactly the same way with FD-SOI since the ultra-thin body of transistors is isolated from the substrate, can be readily transposed in the form of Back-Bias through an ultra-thin BOx. In that scheme, some biasing voltage is applied under the ultra-thin BOx to obtain an effect similar to Body Biasing in Bulk. This kind of approach typically involves implant of n+ or p+ “back-plane” doping right under the BOx for maximum efficiency, as illustrated in Fig. 1-2. of Chapter 1. See also *Ref. [6],* for example.

It is worth noting that recent research *(F.Andrieu, LETI)* indicates back-plane biasing of FD-SOI with UTBOX should be extremely effective, while the expected trend for classical Bulk at nanometer scale geometries is in the opposite direction.

Multi-VT:

Multi-V_T libraries will be built in FD-SOI, but will normally not rely on channel doping modulation, as we are talking here of undoped (or intrinsic channel) FD-SOI devices.

One approach involves tuning of the gate stack work function to shift the V_T (still based on the same metals as High-K Metal Gates of Bulk CMOS though). In that case there is some work at the process and transistor architecture level, but from a designer's point of view that makes no difference.

An alternative approach (which has a lot of synergies with Back-Biasing used as a substitute to Body Biasing) involves tuning the V_T by doping and biasing a back-plane under the BOx of target transistors *(Ref. [7], [8], [9], [5]).* Definition of back-plane implant regions and back-plane contacts has to be taken into account in the layout of transistor level designs (see also *section 4.4*). Then at higher design level, cells from multi- V_T libraries would be used in the same way as with Bulk technologies. Its proponents point out that this is a low cost approach.

A third approach sometimes used at previous technology nodes has been using a set of different channel lengths, to have a choice of different I_{on}/I_{off} operating points. If considering this option, it must be kept in mind that V_T roll-off with FD-SOI is normally less pronounced than with a (virtual) Bulk counterpart, as discussed below.

Channel Length Modulation Techniques:

Techniques such as emulation of multi- V_T with different channel lengths (as touched on in former paragraph) and such as gate length biasing fall in this category. Gate length biasing (or Critical Dimension, CD, Biasing) is a leakage reduction technique that consists of selectively applying, post-layout, a slight increase to gate length of short transistors that are not on critical paths: then these transistors leak less, they are also slower but this is without impact on global chip performance as critical timing paths are not impacted. Channel length modulation can be viewed as excursion on the I_{on}/I_{off} curve of the transistor and is applicable to FD-SOI : longer transistors still leak less than shorter ones. One aspect to bear in mind, however, is that the effect on short transistors is amplified by V_T roll-off. So again the net effect of this technique may not be as strong as expected if expectations ignore the fact that V_T roll-off with FD-SOI is normally less pronounced than with a (virtual) Bulk counterpart. On the other hand, limited V_T roll-off and better variability enable the use of this technique with less dispersion of results.

Besides, it may be worth noting that the tight pitch required by future CMOS technology nodes can make it difficult to apply gate length biasing without violating design rules, especially in Bulk where gate length will be more difficult to scale down than with FDSOI, due to Short Channel Effects.

Conclusion

Going from the availability of an FD-SOI process to a full featured System-on-Chip Integrated Circuit is not expected to require significantly new or exotic design practices. Furthermore, FD-SOI technology can in fact avoid introduction of new design complexity necessary to work around some issues that will arise when scaling traditional Bulk technology to the 22-20nm nodes.

Therefore, developing an FD-SOI ecosystem for the 22-20nm node should not be seen as a daunting task; and in fact could globally represent a work comparable to enhancing the traditional Bulk CMOS ecosystem to support next generation nodes.

In addition, FD-SOI has much to offer to designers in terms of new opportunities to create Area, Power and Performance efficient products with good yields – in other words to give product development teams a leading edge over their competition.

Therefore, from a product and design perspective, the main concern should probably not be: how to design on FD-SOI? but rather: how to ensure access to an efficient FD-SOI technology at the next nodes?

Appendix

Device Availability

FD-SOI will enable technologists to come up with a choice of transistors with very good characteristics for digital and analog applications. However, design of a System-on-Chip involves a number of other devices. Providing them is an issue for technologists rather than designers, however some Full Custom designers will need to be aware of the characteristics of solutions on offer.

Those devices fall in two categories :

- devices that do not involve the Bulk substrate, for example inter-metal capacitors,
- devices that do involve the Bulk substrate, for example some diodes.

Porting the first category to FD-SOI is straightforward. Some devices of the second category can be ported to ultra-thin film FD-SOI, because they simply rely on usage of "active" silicon and thin film is not a problem; however some others cannot be directly ported as they are incompatible with a very thin silicon film. For example, some high voltage devices and bipolar transistors may fall in this category.

It is expected that technology developers, collaborating with designers, will identify the few devices required by the targeted applications that cannot be directly ported, and propose solutions. Two approaches exist. One is to use an alternative device structure: for example, diodes that reach into in the Bulk substrate may be replaced by alternative structures relying on adjacent P and N active areas in the top silicon. The other is to locally etch off top silicon and BOx, thus giving access to the underlying Bulk substrate and enabling a classical Bulk CMOS structure (hybrid Bulk-FDSOI co-integration) to be kept.

Timescales

FD-SOI CMOS technology platform is under development at leading edge technology R&D centers and is on a path to intercept the 22nm/20nm node for mainstream Low Power design. Soitec is already in a position to sample wafers for complete development and qualification of next CMOS node in line with the very tight specifications required to get full benefits of FD-SOI (like top silicon uniformity to be controlled within a few Angstroms), and will be ready to deliver high volumes in 2011. This is in line with requirements for industrial development of a 22nm/20nm FD-SOI Low Power technology over 2010-2012, and could enable retrofit to 28nm. Following the release of industrial compact models fit for simulation of FD-SOI devices; it is anticipated that Design Kit and Library releases will enable commercial IC design to start in the late 2011- early 2012 timeframe (obviously this will also depend on other CMOS challenges, for example scaling of metal interconnects, lithography tools, etc).

References

This is just a short selection of articles that give some background on FD-SOI Technology (on standard BOx or on Ultra-Thin BOx). Many more can be found by checking the references cited in these works.

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[12] - "Low Power Logic and Mixed Signal Technologies",
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