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ESD Sensitivity of 65-nm Fully Depleted SOI MOSFETs with Different Strain-Inducing Techniques

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Presenter Biography

2004	B.S. degree in information engineering (University of Padova, Italy)
2006	M.S. degree in electronic engineering (University of Padova, Italy)
Since January 2007	Ph.D. student at DEI, University of Padova, Italy
2008	visiting student at IMEC (Leuven, Belgium) – Topic: “ESD design and characterization of multigate FinFET devices”

Abstract

The role of this study is to further investigate the ESD sensitivity of new a generation 65-nm Fully Depleted SOI MOSFETs, with particular attention to the strain engineering. The focus is on the devices that need to be protected from ESD, rather than on the protection structures themselves.

A detailed electrical investigation is carried out in order to classify the observed failure modes and mechanisms. We propose a new failure criterion based on sub-threshold drain current that allows us to univocally identify the device failure (i.e. filament between source and drain and/or gate-oxide breakdown).

Finally, we show that the failure voltage depends on the strain level and the gate length, indicating that the strain-engineering may have a non-marginal impact on the reliability of advanced CMOS devices. Furthermore, we show the absence of filament in sCESL+SOI MOSFETs.

Outline

- **Motivations**
- **Purpose of the work**
- **Experimental and devices**
- **Failure voltage criterion**
- **The role of the strain engineering**
- **Conclusions**
- **References**

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Motivations

- Simple shrinking is no longer sufficient to continue with the **CMOS scaling**

Solutions:

- ✓ **Silicon On Insulator (SOI) technology**
 - ✓ **Strain engineering**
-
- **ESD** could be a **major concern for SOI devices**

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Purpose of the work

- Investigate the **ESD sensitivity** of **65-nm Fully Depleted SOI MOSFETs**, with particular attention to the **strain engineering**
- The **focus** will be on the **devices that need to be protected from ESD**, rather than on the protection structures themselves

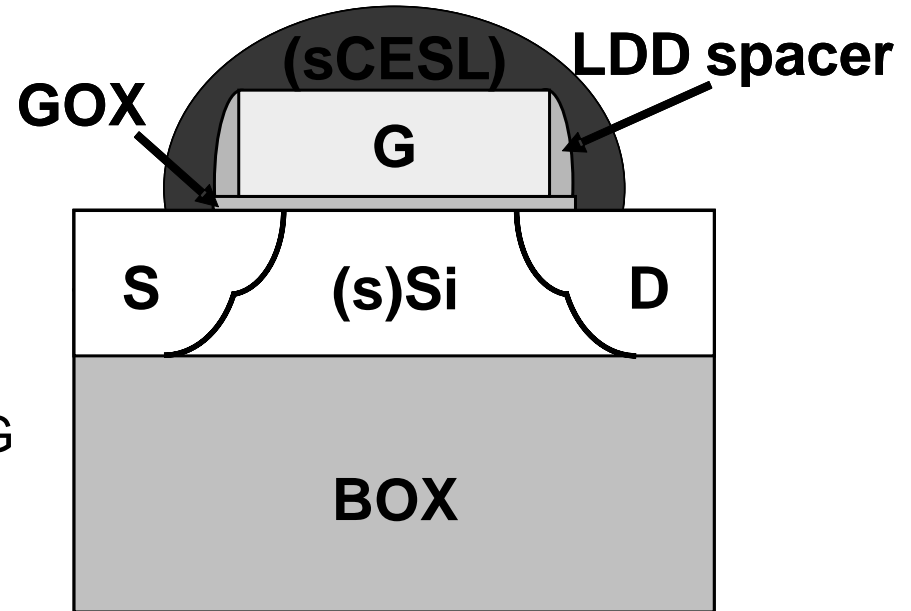
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Experimental and Devices

65-nm FD SOI MOSFETs:

- $t_{\text{OX}} = 1.5 \text{ nm SiON}$
- $t_{\text{Si}} = 15 \text{ nm (undoped)}$
- $t_{\text{BOX}} = 150 \text{ nm}$
- $W = 10 \text{ }\mu\text{m}$ and varying L_G



Three variants were processed:

- 1) SOI: Si substrate
- 2) sCESL+SOI: additional tensile SiN layer
- 3) sSOI: SiGe substrate

Experimental and Devices

- Stress conditions:
 - ✓ **GGMOS** configuration
 - ✓ by means of an on-wafer TLP-like system

- **After each pulse** the drain leakage current and **a full set of device DC characteristics** were measured

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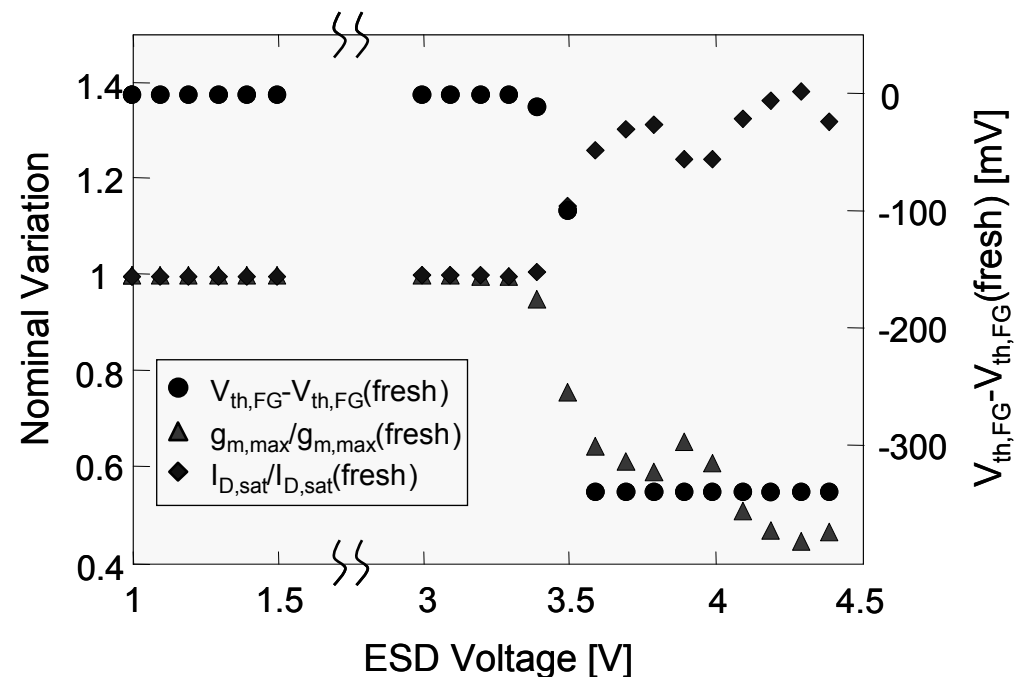
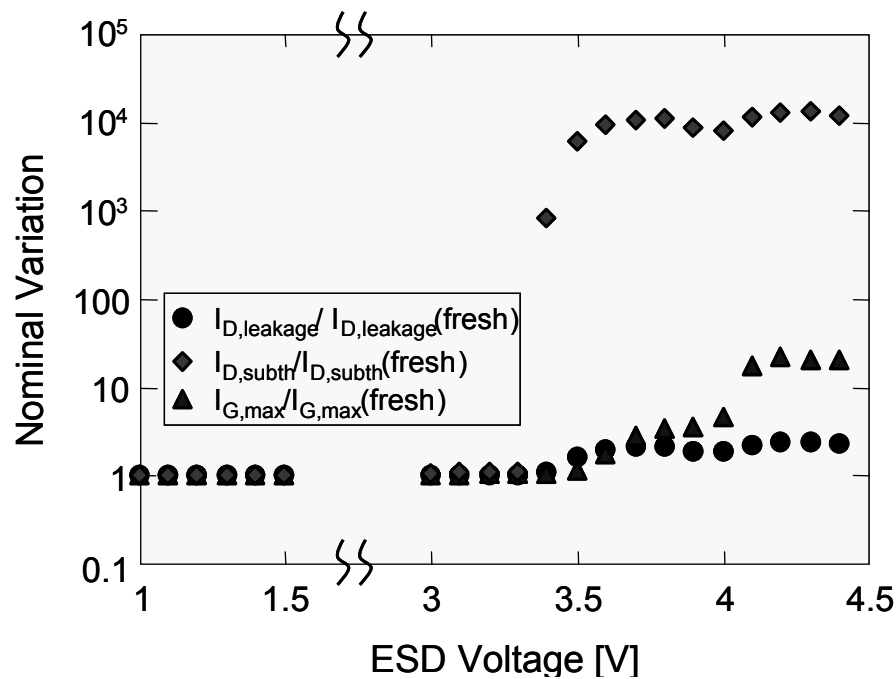
Failure voltage criterion

- **Usually:**
device failure = a large change occurs in I_{leakage} of the terminal subjected to the ESD
- **In this work:**
full set of measurements of the DC characteristics (after each ESD step)

Failure voltage criterion

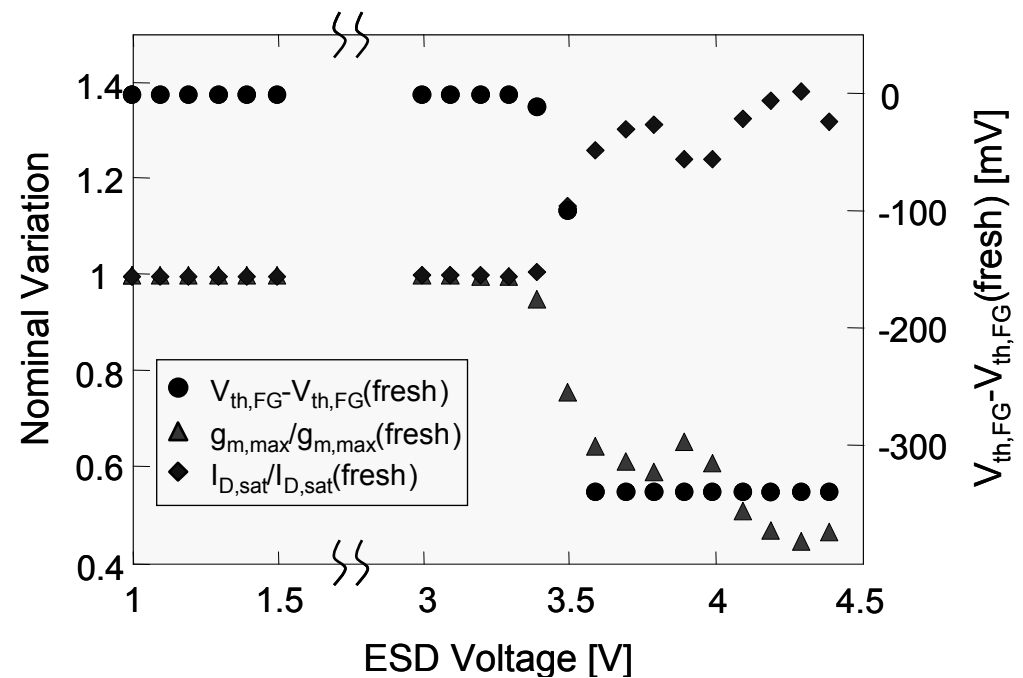
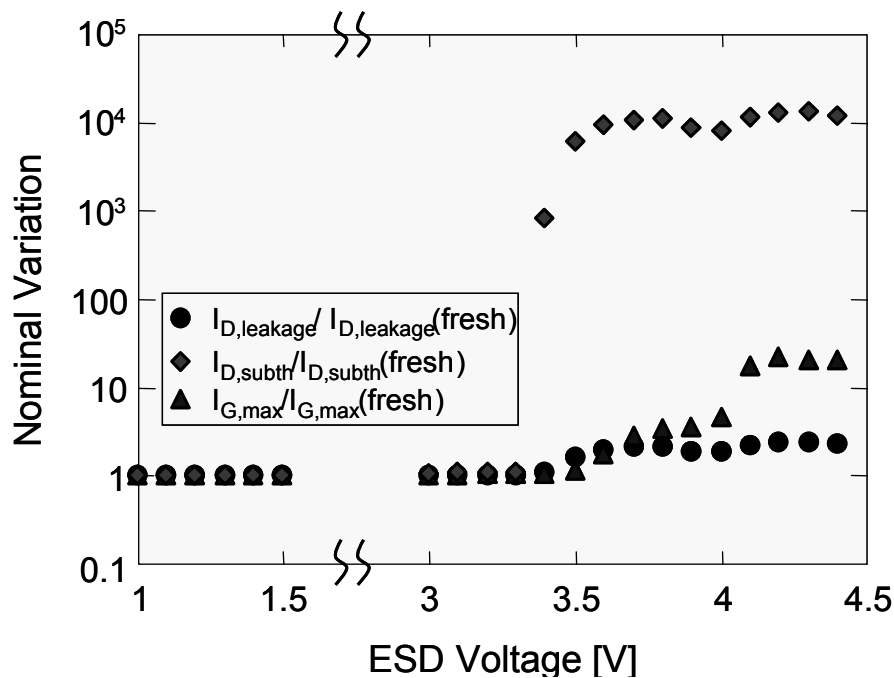
Two regions:

1. $V_{DS} < 3.4$ V: all parameters are unchanged
2. $V_{DS} \geq 3.4$ V: the parameters vary



Failure voltage criterion

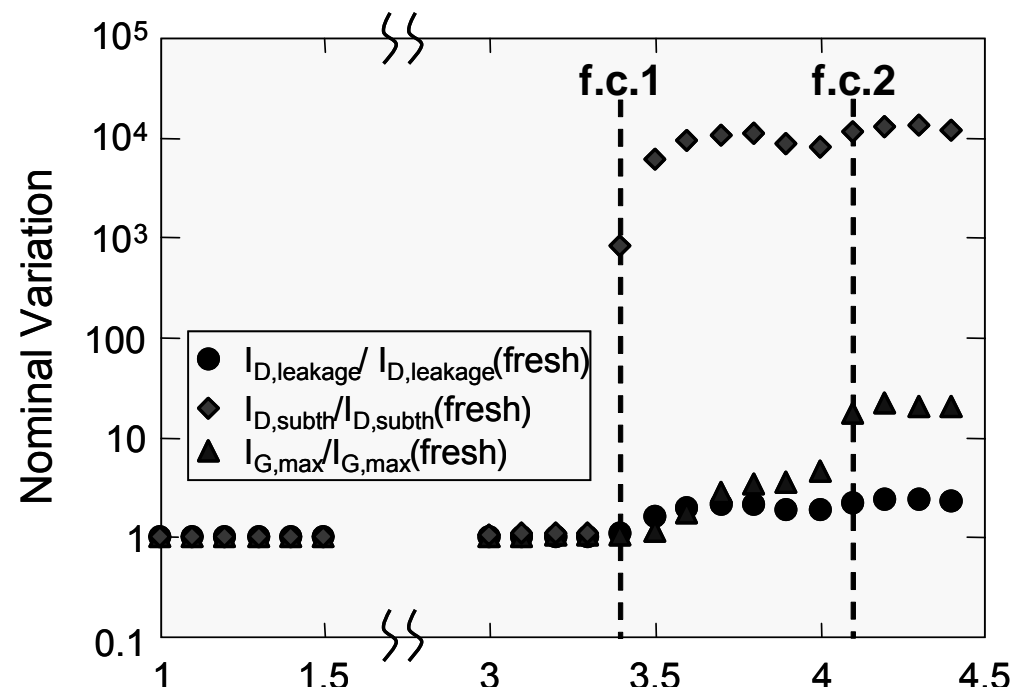
$I_{D,subth}$ (@ $V_{GS} = -0.75$ V, $V_{DS} = 25$ mV, $V_{BS} = 0$ V) experiences the **larger variation** (> 100 times), while the other parameters show smaller variations



Failure voltage criterion

Two failure criteria:

- 1) **f.c.1: $I_{D,\text{subth}}$ variation > 10 times**
- 2) **f.c.2: $I_{G,\text{max}}$ variation > 10 times**

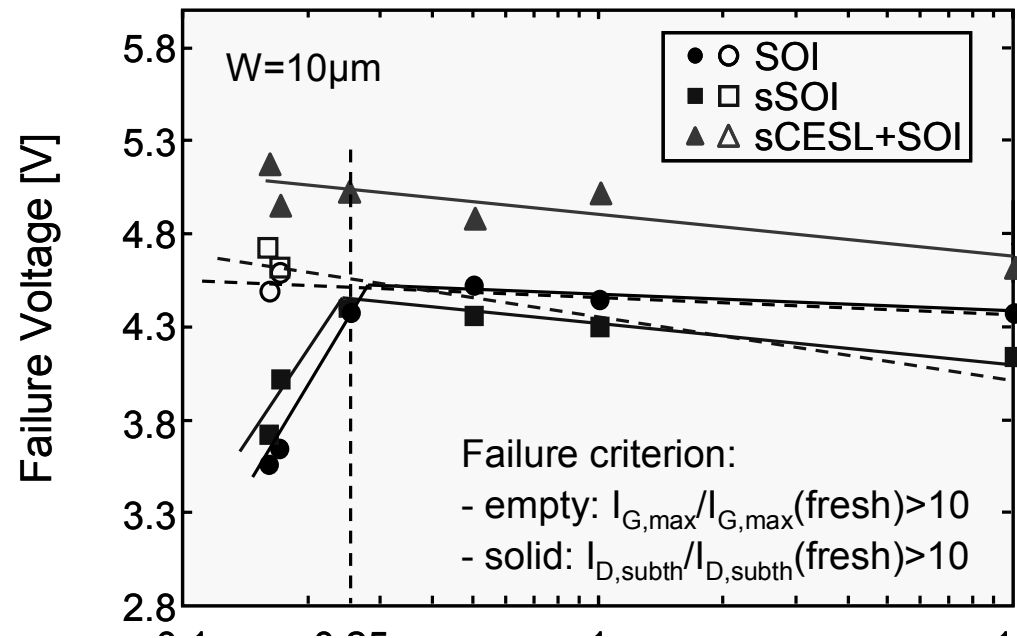


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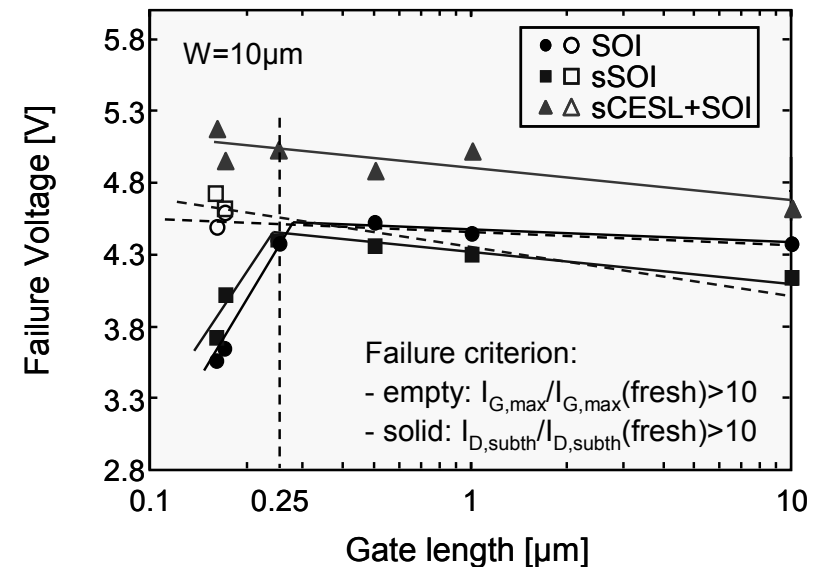
The role of strain-engineering

- **sCESL+SOI: V_{failure} vs L is independently of the adopted f.c.**
- **SOI and sSOI: V_{failure} vs L depends on the chosen f.c.**



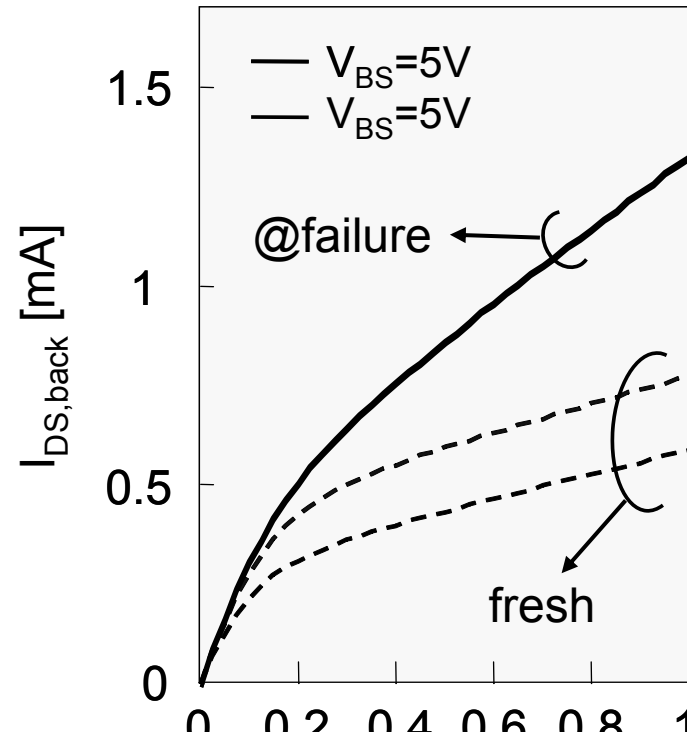
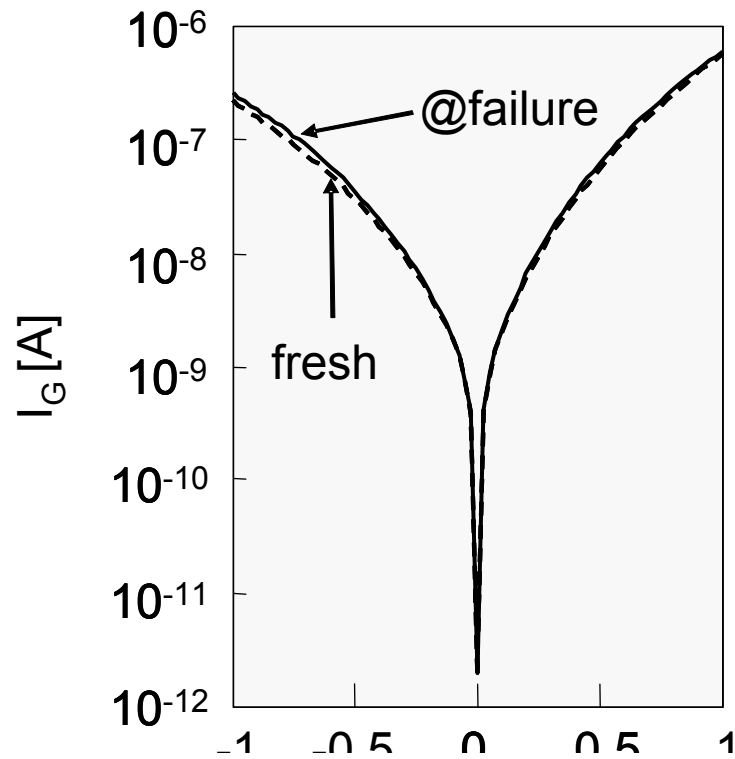
The role of strain-engineering

- **f.c.1** is reached **before f.c.2** in SOI and sSOI MOSFETs
- **filament** (extra $I_D \sim 100$ nA) is likely to occur **before GOX breakdown**
- **f.c.1** is sensitive to filaments formation (filament current adds to $I_{D,subth} \sim$ nA)
- **f.c.2** is sensitive to gate-oxide breakdown (extra $I_G \sim 100$ μ A)



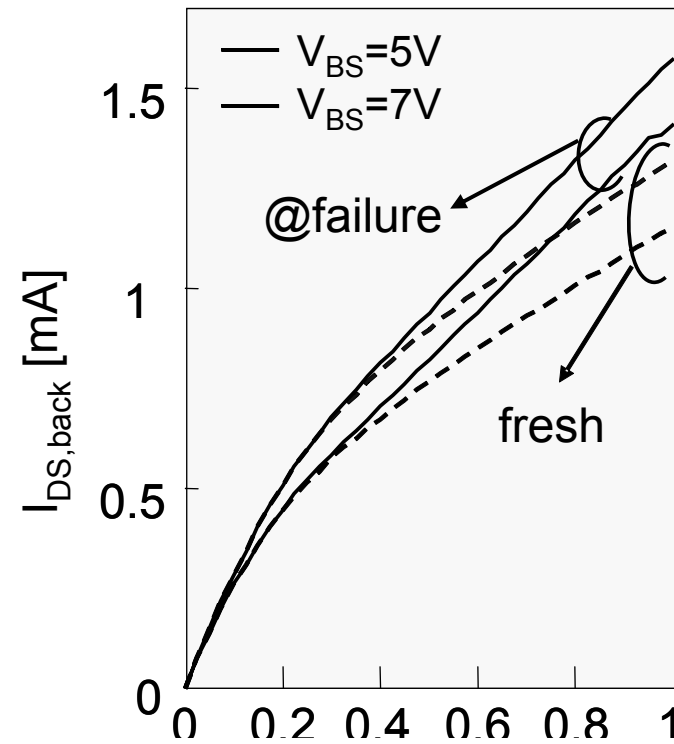
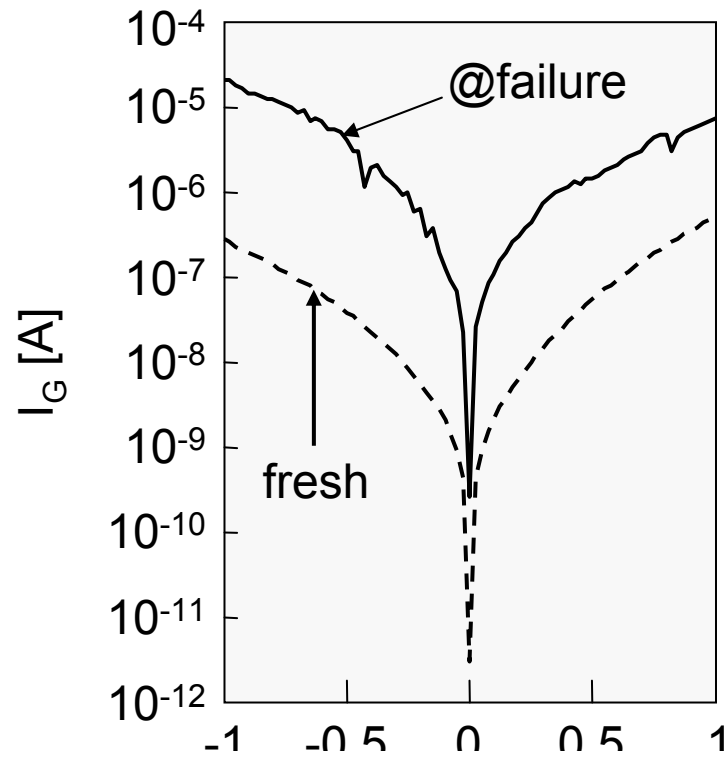
Short-Channel SOI and sSOI MOSFETs

Creation of a conductive path between source and drain (**filament**) possibly located near the Si/GOX interface



Short-Channel sCESL+SOI MOSFETs

- **GOX breakdown**
- sCESL may prevent the melted material to move along the channel inducing the filament



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Conclusions

We have demonstrated:

- a valid failure criterion is given by the sub-threshold current, indicating when the filament and/or the GOX breakdown occurs
- the failure voltage depends on the strain level and the gate length

The strain-engineering may have a non-marginal impact on the reliability of advanced CMOS devices

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References

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