

Material aspects and challenges for SOI**FinFET integration (invited)**

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Multi-gate MOSFETs are the most promising approach to address short channel effects and leakage issues in deeply scaled CMOS because of their better electrostatic gate coupling to the channel compared to planar bulk MOSFETs [1]. Moreover, ultra-thin-body fully-depleted devices eliminate the need for channel doping, thereby reducing parametric spread due to dopant fluctuations and reducing junction leakage due to high electric fields. One of the leading multi-gate candidates is the Fin Field-Effect-Transistor, FinFET [2,3]. A trigate FinFET device consists of a vertical standing Si body (fin) and the gate is wrapped around either side creating two channels on the sides and one on the top (Fig.1). An important advantage of the FinFET is that gates are self-aligned and can be fabricated with a single lithography and etch step. High-aspect-ratio trigate FinFETs with aggressively scaled fin widths (10 nm and narrower) are of particular interest as they combine excellent SCE immunity with high drivability per unit chip area.

In this work, we will elaborate on the key material aspects of front-end-of-line Silicon-On-Insulator (SOI) trigate FinFET integration with high fin aspect ratio. We will discuss the different processing step from a materials research perspective such as fin patterning, gate stack deposition and gate patterning. The 3D configuration of a FinFET poses a key challenge for FinFET integration, i.e. the fabrication of low-resistive contacts to the channel. The regions that contribute to series resistance of device are: the extension region, the source/drain (SD) region and the silicide. All these regions are geometrically different in a FinFET compared to a conventional bulk MOSFET and therefore require modified integration schemes. It will be shown that the formation of low-resistive contacts including extension, selective epitaxial growth (SEG) on the fin source/drain areas (Fig. 2), optimized source/drain implants and silicidation conditions are paramount to achieve low access resistance (Fig. 3) and high drive currents. For instance, SEG decreases the access resistance of FinFET transistor, R_{SD} , when SEG is formed on S/D regions, while the use of amorphising implant can lead in an increase in R_{SD} for narrow fins [3] (Fig. 3).

- [1] H.-S. P. Wong, D.J. Frank, P. M., C. H.J. Wann, and J. J. Welser, "Nanoscale CMOS," Proc. IEEE, vol. 87, pp. 537-570, April 1999.
- [2] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-A self-aligned double-gate MOSFTE scalable to 20 nm," in *IEEE Trans. Electron Devices*, vol. 47, pp. 2320-2325, Dec. 2000.
- [3] M. J. H. van Dal *et al.*, "Highly manufacturable FinFETs with sub-10nm fin width and high aspect ratio fabricated with immersion lithography," *Symp. VLSI Tech. Dig.*, 2007, pp. 110-111.

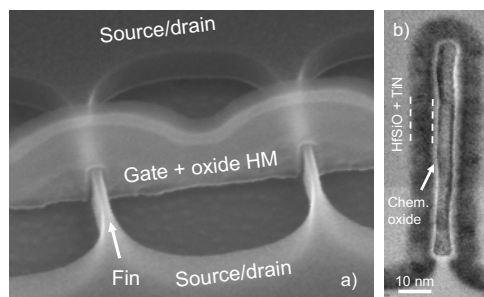


Figure 1. a) Tilted top view SEM image of FinFET device after gate patterning.; b) TEM cross-section of a FinFET perpendicular to the current flow with a 5nm wide, 65 nm tall fin (aspect ratio 13). The gate stack consisted of a HfSiO gate dielectric and TiN metal gate.

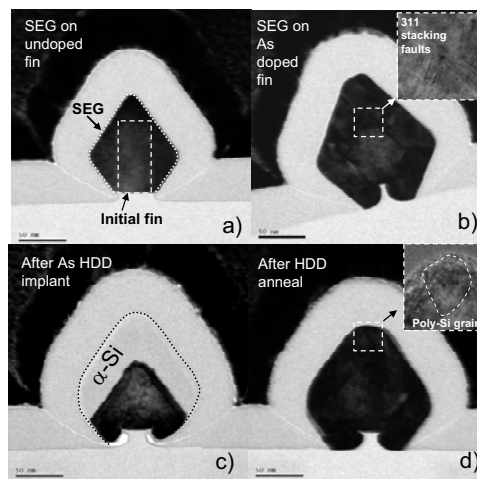


Figure 2. TEM cross-sections of a fin showing the SEG Si integrity on: a) undoped fin, b) As 5keV 1e15 doped fin (implant prior to SEG), c) HDD implant (As 25 keV + P 8 keV) (implant after SEG), and d) same as (c) with activation anneal at 1050°. SEG growth and Si integrity is affected by implant conditions.

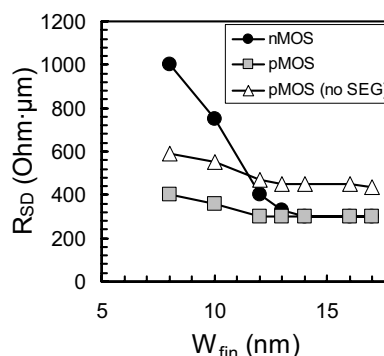


Figure 3. FinFET access resistance R_{SD} as a function of W_{fin} for nMOS with SEG and pMOS devices with and without SEG. R_{SD} was extracted by extrapolating the on-state resistance R_{on} (measured at $V_{g,on} = 3$ V) versus L_g plot to $L_g = 0$.