Evidence for Substrate Bias Effects in SOI ΩFETs

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1. Abstract

It is generally accepted that, due to strong coupling of the lateral gates, narrow SOI Multiple-Gate FETs (MuGFETs) are immune to substrate effects [1]-[3]. Nevertheless, in this work we present experimental evidence for significant substrate bias effects in narrow SOI ΩFETs, consisting in the strong variation of the drive current, transconductance and gate-induced drain leakage current (GIDL), with invariant threshold voltage, subthreshold slope and DIBL. The origin and possible implications of the observed effects are discussed.

2. Introduction

The MuGFET is known as the most promising device architecture for nano-scaled CMOS technologies [1]–[3]. The multiple-gate structure and a thin (narrow-fin) Si body provide a strong electrostatic gate control of the potential in the body, suppressing short-channel effects [4],[5]. Next to that, the strong gate coupling of the lateral gates greatly reduces the back-gate influence in narrow-fin SOI MuGFETs [1]-[3]. It has been shown that, in Ω-gate FETs with very narrow fins, the threshold voltage, subthreshold slope and DIBL are virtually unaffected by back-gate or substrate bias [3]. The purpose of this work is a further investigation of the substrate effects in MuGFETs, using extensive measurements, with the emphasis on narrow ΩFETs. We experimentally demonstrate that, in *short-channel* narrow ΩFETs, substrate bias can dramatically change the on-current, transconductance and GIDL, which is attributed to modulation of the electric field and carrier distribution in the source/drain extensions and gate-to-extensions overlap regions. These effects should be taken into account in the predictions of the MuGFET's reliability and performance. They can be used for diagnostics of advanced MuGFETs.

2. Device Description

ΩFETs have been fabricated on SOI substrates. The fabrication process is described in [6],[7]. The gate stack consisted of a nitrided oxide with 1.8 nm EOT and MOCVD TiN, capped with 100nm poly-Si. High angle As implantation was used to dope the extensions and 45 nm PECVD nitride spacers were formed. No SEG was used to reduce the S/D resistance. After spacer etch, As+P HDD implantations were done, followed by a 1050^0C spike anneal and a standard NiSi process. The measured devices are undoped-channel 5-fin NMOSFETs. The fin height H_{fin} is 60 nm, and the buried oxide thickness is 145 nm. The fin width W_{fin} varies from 1 μm down to 25 nm. The gate lengths L_g from 10 μm down to 40 nm are considered.

4. Measurement Results and Discussion

The drain current I_d and transconductance g_m were measured as a function of the gate voltage V_g for various substrate biases V_{sub}. Measurements at low V_d for different gate lengths L_g are presented in Figs.1 and 2. For W_{fin}=25 nm a change in V_{sub} from –40 V to +40 V does not cause any change in subthreshold slope S and threshold voltage V_{th} (logarithmic-scale $I_d(V_g)$-curves in Fig.1(a-c), Fig.2 (a)), as expected for narrow-fin ΩFETs [3]. However, V_{sub} causes a change in the on-current I_{on}, which is evident from the linear-scale $I_d(V_g)$-curves in Fig.1(a-c). This change strongly depends on L_g. It is only faintly visible for L_g=10 μm, whereas it is rather pronounced for L_g=1 μm, and becomes very large for L_g=80 nm. In the 80-nm-long narrow-fin device, g_m also strongly varies with V_{sub} (Fig.1 (d)). This variation of g_m and I_{on} is reduced in the devices with larger W_{fin}, in which the back-gate induced V_{th}-shift is however more pronounced (Fig.2).

Similar features, namely, strong variation of I_{on} and g_m with V_{sub} without noticeable change of V_{th} and S are observed in narrow-fin 80-nm-long devices at high V_d (Fig.3). DIBL is also unaffected by V_{sub} for both W_{fin}=25 nm and W_{fin}=35 nm (insets in Fig. 3(c, d)). However, V_{sub} has a pronounced effect on GIDL, and this effect is much stronger for W_{fin}=35 nm than for W_{fin}=25 nm (Fig.3 (c, d)).

Insensitivity of S, V_{th} and DIBL to V_{sub} in our narrow-fin ΩFETs suggests that the observed V_{sub}-effects are not related to the variation of the potential in the channel region or at the channel edge. Indeed, as is evident from Fig. 4(a), in strong inversion the variation of the total resistance $\Delta R_{tot}(V_{sub})$ in the 80-nm- and 1-μm-long devices is exactly the same, indicating that the observed V_{sub}-effects are not related to the channel region, rather they are due to regions outside the channel. Most probable reason seems to be modulation of the extensions series resistance R_s. Fig.4(b) shows R_s as a function of V_{sub} extracted using $I_d(V_g)$-measurements at low V_d on the long-L_g devices with different L_g (1-10 µm). One can see that R_s strongly changes with V_{sub}. For W_{fin}=25 nm, change in V_{sub} from –40 V to +40 V reduces R_s nearly by half. This is rather surprising, since our devices have heavily-doped extension regions (~10^{20} cm^{-3}) and a conventional gate-overlapped structure. It may be caused by incomplete activation of the dopants, dopant loss and increased extent of amorphization in narrow-width extension regions, resulting in a lower electrically active doping concentration in real devices [8]. The variation of GIDL with V_{sub} can be attributed to modulation of the electric field in the gate overlap region, and its suppression for reduced W_{fin} can be explained by an increased role of the internal gate fringing field.

4. Conclusions

We have presented experimental evidence for significant substrate bias effects in short-channel narrow ΩFETs. One is the drastic change of the on-current and transconductance attributed to modulation of the extension resistance. Another effect is the variation of GIDL attributable to a change of the electric field in the overlap region. This means that short-channel narrow ΩFET can be sensitive to parasitic substrate effects (hot-carrier, radiation effects, etc). Since the observed effects are rather sensitive to actual doping profiles in the extensions and overlap regions, they may be helpful in diagnostics of advanced MuGFETs, taking into account that it is very difficult to predict 3D dopant profiles in real MuGFETs. Furthermore, they should be considered in the predictions of the MuGFET's true performance potential determined by the drive current.

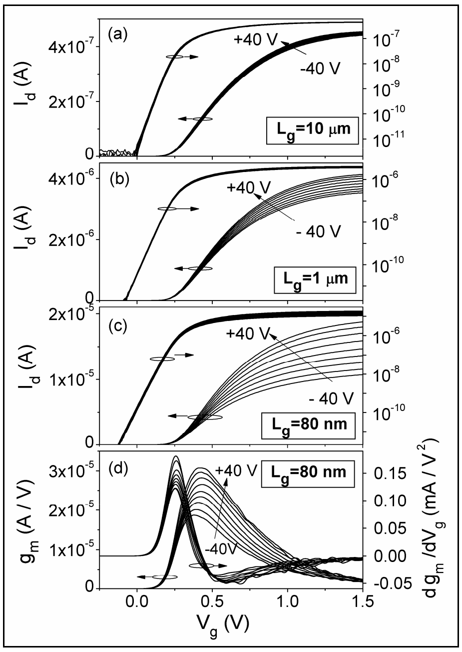

Fig.1: *Effect of V_{sub} on the transfer characteristics in linear and log scales in ΩFETs with W_{fin}=25 nm and different L_g: (a, b, c); (d) first and second derivatives of $I_d(V_g)$-curves for L_g=80 nm, showing variation of g_m and invariability of V_{th}.*

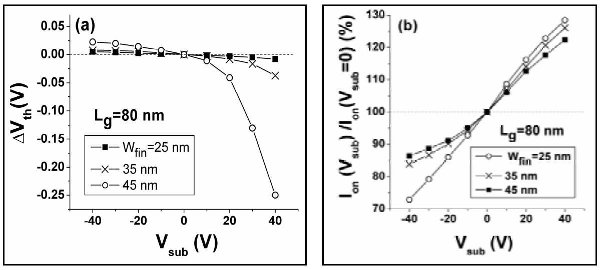

Fig.2: *Variation of the threshold voltage and on-current as a function of substrate bias (relative to those at V_{sub}=0) in the devices with L_g=80 nm and various fin widths (V_d=20 mV).*

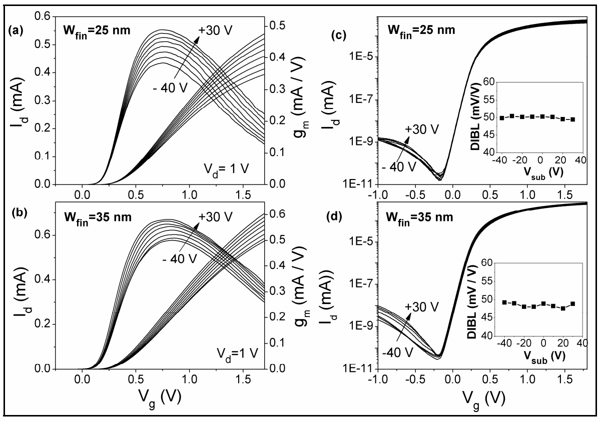

Fig.3: *Transconductance and transfer characteristics for 80-nm-long ΩFETs at V_d=1 V for various V_{sub}: (a. c) W_{fin}=25 nm, and (c, d) W_{fin}=35 nm. Insets in (c, d) show DIBL versus V_{sub}.*

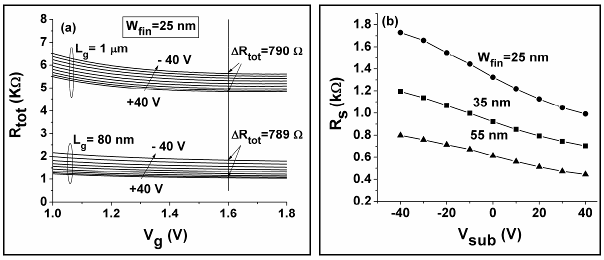

Fig.4: *(a) Total resistance in strong inversion for various V_{sub} in 80-nm-long and 1-µm-long devices with 25-nm-wide fins. (b) Series resistance as a function of substrate bias for various fin widths, extracted from long-L_g device measurements.*

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