# Junctionless MuGFETs

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## 1. Abstract

This paper describes the simulation of the electrical characteristics of a new transistor concept called "Junctionless MuGFET". The proposed device has no junctions, a simpler fabrication process, less variability and better electrical property than classical inversion-mode devices with S&D PN junctions.

## 2. Introduction

Research in multi-gate SOI MOSFETs (MuGFETs) for deep submicron CMOS applications is currently being carried out by many semiconductor companies, as these devices hold the promise for pushing the limits of silicon integration beyond the limits of classical planar technologies [1]. In a MuGFETs the gate electrode is wrapped around a silicon wire, called "finger" or "fin", forming a multi-gate structure with excellent control of the channel potential (fig. 1). The excellent gate-to-channel coupling allows one to fully deplete the channel region even if it is heavily doped (fig. 2 (a)). In very short-channel devices (*L*=10nm or less) it becomes quite difficult the formation of S&D junctions is quite a challenge and imposes drastic conditions on doping techniques and thermal budget. The devices proposed here are fabricated without source and drain implantation process. We also show that these junctionless devices have better electrical characteristics than conventional inversion-mode devices (fig. 2 (b)).

## 3. Device simulation

The schematic structure of MuGFETs is shown in figure 1. The electrical characteristics of the devices were simulated using the Atlas 3-D device simulator [2]. The simulated structures have a uniform doping concentration in the channel and source/drain regions. Abrupt source and drain junctions are used. Table 1 shows parameter of simulated devices.

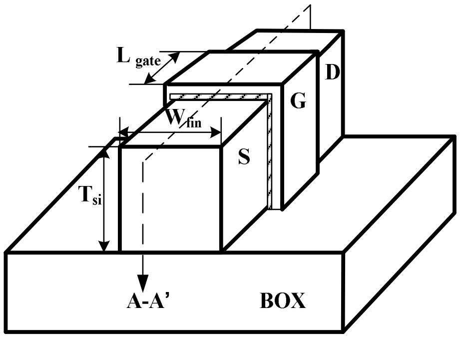

**Fig.1:** *MuGFET device schematic view.*

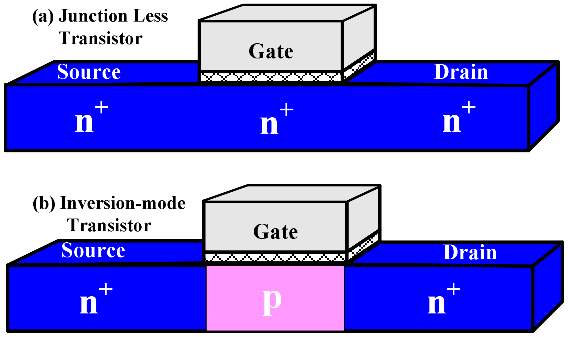

**Fig.2:** *Cross-section view of figure 1 A-A'.*
*(a) Junctionless device (b) Inversion-mode device.*

| | Inversion-mode | Junctionless |
|---|---|---|
| Channel Doping | $2\times10^{15}cm^{-3}$ (P) | $8\times10^{19}cm^{-3}$ ($N^+$) |
| Gate oxide thickness | 2nm | 2nm |
| Gate workfunction | 4.6eV | 5.5eV |
| $T_{si}$ | 5nm | 5nm |
| $W_{fin}$ | 5nm | 5nm |
| $L_{gate}$ | 5nm to 30nm | 10nm to 30nm |

**Table.1:** *MuGFET device parameters.*

## 4. Simulation Results

Figure 3 shows simulated *I-V* characteristic of junctionless devices for different gate workfunction values. The device requires a high-workfunction gate material, such as $P^+$ polysilicon or platinum, to achieve a suitable $V_{TH}$ value.

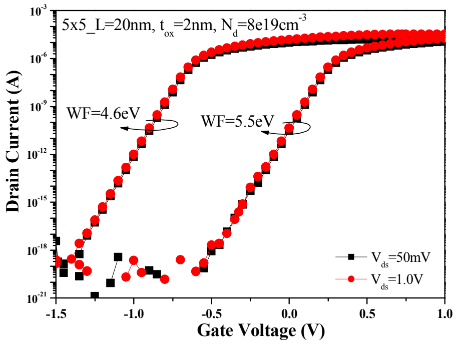

**Fig.3:** *I-V characteristic of Junction-less device with different gate workfuction at $L_{gate}$=20nm.*

We compared electrical characteristic of junctionless and classical Inversion-mode devices as shown in figure

4. In this paper we used a lightly doped channel for inversion-mode devices to avoid corner effects [3]. The simulated inversion-mode devices have a source/drain and source/gate overlap of 1nm, which means that effective channel length of the device is 8nm when the physical gate length is 10nm. One can see that the junctionless MuGFET has better subthreshold slope and *DIBL* characteristics than inversion-mode devices.

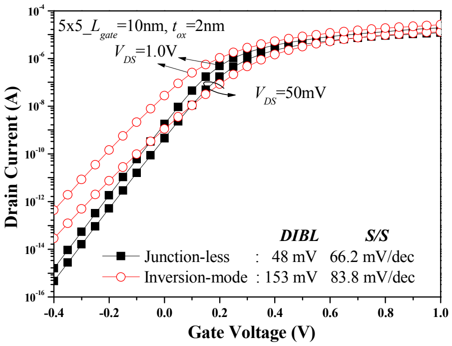

**Fig.4:** *I-V characteristic of Junction-less device and Inversion-mode device with $L_{gate}$=10nm.*

The simulated results for *DIBL* and threshold voltage versus physical gate length for both junctionless MuGFETs and inversion-mode MuGFETs are plotted in figure 5. The *DIBL* is defined as the difference in threshold voltage when the drain voltage is increased from 0.05V to 1.0V (*DIBL* = $V_{th}(V_{DS}$ = 0.05 V) - $V_{th}(V_{DS}$ = 1 V)). The junctionless MuGFETs has better short-channel characteristics than inversion-mode devices. In this simulation, the overlap length of the inversion-mode device is 1nm.

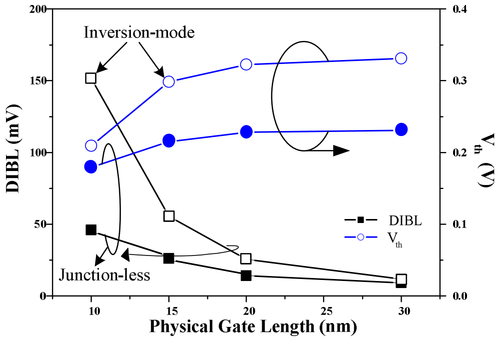

**Fig.5:** *DIBL and threshold voltage of Junction-less and Inversion-mode device as a function of physical gate length.*

Figure 6 shows simulated threshold voltage of inversion-mode MuGFETs as a function of effective channel length with $L_{gate}$=10nm at $V_{DS}$=50mV. We defined the effective channel is junction length of between source and drain. One can see a variation of the threshold voltage in inversion-mode devices is large due to the resistance of the gate overlap/underlap region [4] while the threshold voltage of the junctionless device is insensitive to effective channel length. Therefore the junctionless device is more insensitive to process variations than regular devices.

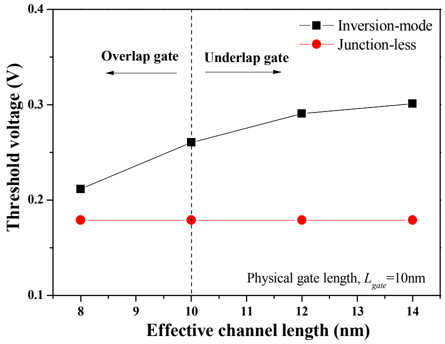

**Fig.6:** *Threshold voltage of inversion-mode device as a function of effective channel length at $V_{DS}$=50mV*

Figure 7 shows subthreshold characteristics of junction-less MuGFETs with different $L_{gate}$ values (5nm-20nm) at low drain voltage. The subthreshold slope of shortest gate length of junction-less device is below 80mV/dec. This shows the potential of junctionless transistor for extremely short-channel applications.

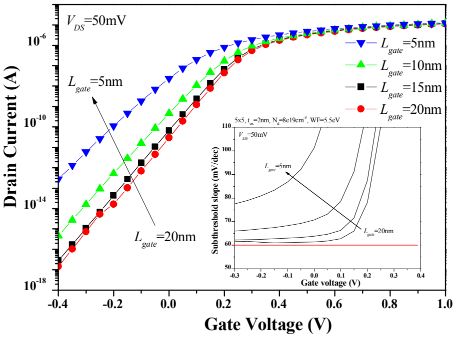

**Fig.7:** Subthreshold characteristics of junctionless devices with different physical length.

## 5. Conclusions

In this paper, we proposed good electrical characteristics of new MuGFETs device concept. The performances of junction-less and inversion-mode multigate FETs are compared. The proposed device is more stable with process variation and has better electrical properties than inversion-mode devices.

## Acknowledgements

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## References

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