

# 3D simulation of Nanowire by Full-Real Space NEGF Simulator

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## 1. Abstract

In this article, we present the effects of device parameters variations on the electrical characteristics of rectangular Nanowire. Our three dimensional (3D) device simulator is based on the Non Equilibrium Green Function (NEGF) formalism. Starting from a basic structure GAA Nanowire with a gate length of 10 nm, variation of gate length and channel thickness was carried out in connection with the numerical calculation of device characteristics. In this work Quantum transport equations are solved in 3D by NEGF method in active area of the device to obtain the charge density and Poisson's equation is solved in entire domain of simulation to get potential profile.

## 2. Introduction

Current technology pushes device dimensions toward limits where the traditional semiclassical Boltzmann theory can no longer be applied and full quantum mechanical approaches which describe the quantum transport in nanostructures are required. Recently reported device structures have metal-oxide semiconductor (MOS) channel lengths in the order of 10 nm or even smaller. Multigate devices and other nanowire transistors are considered to be the promising candidate for the nanoscale regime. Numerical device simulation is an important procedure for the design and optimization of such novel semiconductor devices. Advantages are the calculation of the electrical behavior before the fabrication process, the calculation and visualization of values such as the carrier concentration profile and the potential distribution inside a device.

## 3. Device simulation

The simulation procedure consists in solving the Poisson and NEGF equations self-consistently until convergence is reached. NEGF equation is solved by discretizing the 3D effective-mass Hamiltonian using a Finite Difference Method (FDM). We have used COMSOL MultiPhysics® Software to solve the 3D Poisson equation. This package uses the finite element method (FEM) with irregular mesh to solve the Poisson's equation. We have parallelized the quantum transport equation using Message Passing Interface (MPI) and run it on the SFI400 UNIX Cluster available in the Tyndall National Institute. Neglecting the communication overhead between CPUs we got a linear

speed up of the solver with the number of CPUs used. Details about numerical implementation of NEGF formalism can be found in the literature.

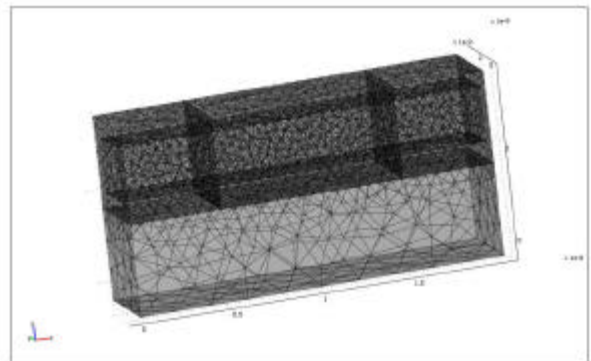
## 4. Simulation Results

Figure 1 shows the schematic structure of Triple-Gate rectangular Nanowire created by COMSOL MultiPhysics®. The NEGF mesh can be chosen to be uniform or non-uniform depending on the problem at hand. Figure 2 shows the 3D electron density in the nanowire at saturation. Figure 3. Shows the potential profile cut in the middle of the device (not in saturation). Figure 4 shows the I-V characteristics for triple-gate Nanowire with different silicon thicknesses/width ( $W_{si}=T_{si}$ ). the variations of different electrical characteristics such as  $I_{off}$ ,  $V_{th}$  and subthreshold swing ( $SS$ ) can easily be derived from this graph. Figure 5 shows the transmission versus energy for different silicon thicknesses. One can see that as the thickness increases the number of energy level increases and the separation between subbands become smaller.

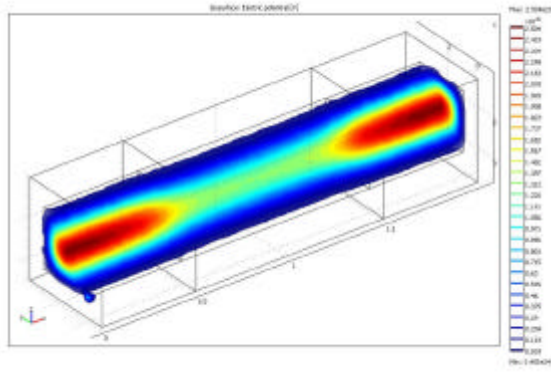
Figure 6 shows the efficiency of the parallel algorithm. In calculating the efficiency we have neglected the communication time between CPUs and other parameters. In general, we have defined the efficiency as follow:

$$Speedup/ Efficiency = \frac{Time\_serial(1\ CPU)}{Time\_parallel(1\ CPU)}$$

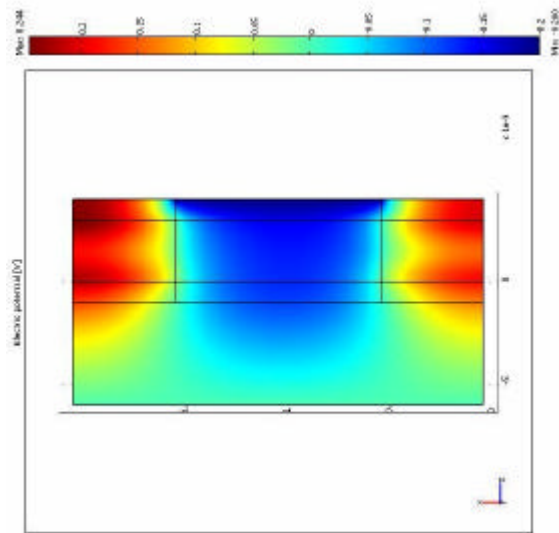
Where the serial and parallel times are the time spent in the Recursive algorithm only.



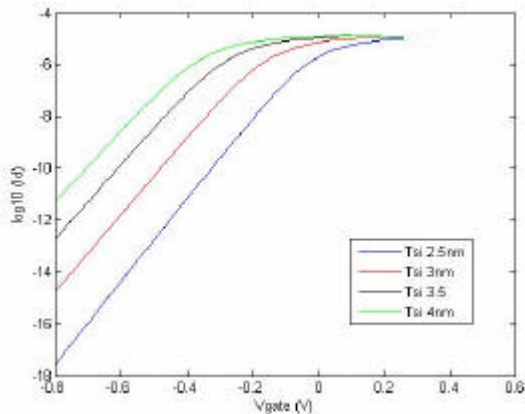
**Fig.1:** Schematic view of Silicon Nanowire Transistor. The irregular mesh in the geometry is generated by COMSOL MultiPhysics® to solve Poisson equation.



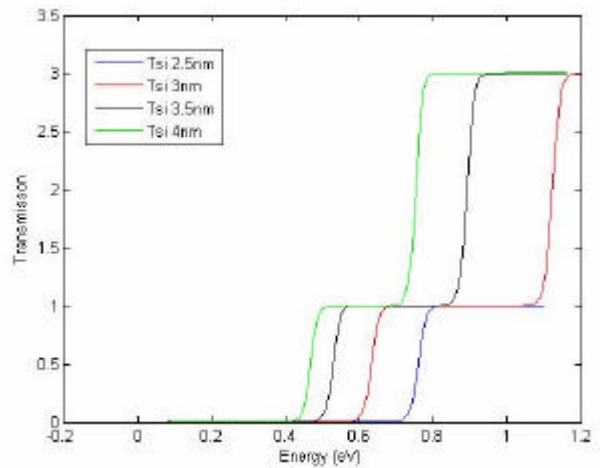
**Fig.2:** Three dimensional Electron Density in the active region of TripleGate Nanowire Transistor with 3nm cross section.  $V_G=?$  and  $V_D=?$



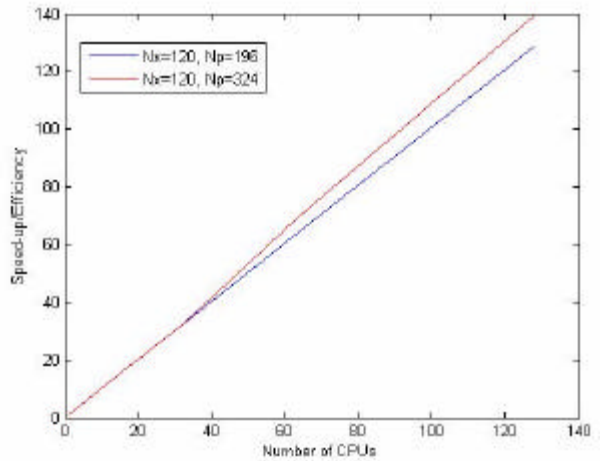
**Fig.3:** Potential profile cut in the middle of the device with  $T_{si}=3nm$ ,  $V_{ds}=0.05 V$ .



**Fig.4:** I-V characteristic Triple\_Gate Nanowire device with  $L_{gate}=10nm$  and variable Silicon Thickness. The variation of  $I_{off}$ ,  $SS$  and  $V_{th}$  can easily be seen from this graph.  $V_D=?$



**Fig.5:** Transmission Vs Energy for Nanowire with different cross-section. The number of subbands and their spacing varies with silicon thickness.



**Fig.6:** Speedup/efficiency in parallelizing RGF algorithm over energy space. It is clear that almost a linear efficiency can be achieved neglecting the time required to communicate between CPUs.

## 5. Conclusions

In this paper, we have shown the development of three dimension real-space Device simulator based on Non-equilibrium Green Function formalism. Furthermore we parallelized the simulator in order to be fast and be able to simulate large device structures. The speed and numerical stability of the simulator has been verified by applying it to different Nanowire device structures.

## Acknowledgements

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## References

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