

Quantization effect in Capacitance Behavior of Nanoscale Si MuGFETs

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1. Abstract

An unusual bump in the gate capacitance characteristics of Si nanoscale MuGFETs is presented and explained here through 3D NEGF quantum simulations. As higher order subbands are populated when the gate voltage is increased, the channel moves closer to the surface. This increases the slope in the I_d - V_g and creates the bump in the $C_g(V_g)$ curve as the centroid of the charge moves closer to the Si/SiO₂ interface and the capacitance is increased.

2. Introduction

In a continuous effort to increase current drive and better control short-channel effects, device dimensions are shrunk. As well, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multigate structure. For ultra-scaled devices with cross-section dimensions smaller than 10 nm and channel length, L , of a few nanometers to a few tens of nanometers, quantum effects are playing a crucial role on device performances and parameters. Here the impact of these effects on the gate capacitance of nanoMOSFETs, which is a major figure of merit to evaluate their performances, is studied through 3D NEGF quantum simulations [1].

3. Simulation results and interpretation

The gate capacitance, C_g , behavior of ultra scaled devices is expected to be strongly influenced by quantum effect [2,3]. In [2], a bump in the $C_g(V_g)$ curve is predicted in carbon nanotubes (CNT) simulations. These have a diameter of a few nanometers and the bump is related to the particular 1D subband structure and density of state (DOS) of the CNT. The DOS can indeed decrease locally for increasing V_g , due to the unavailability of states around the Fermi level, E_F , in between two subbands. This in turn influences C_g , through one of its series component: the semiconductor capacitance C_S which is proportional to the density of states (DOS) at Fermi level [3]. This effect was not predicted in silicon nanowires of similar diameters and no discontinuities were present in the simulated V_g range. Indeed, in silicon, the DOS was not reduced. Furthermore, C_S was rapidly exceeding the two other series component in C_g , *i.e.* C_{ox} , the constant oxide capacitance, and C_d , the depletion capacitance, which renders the gate capacitance insensitive to C_S variations.

In Si nanowires, on the other hand, C_g is strongly influenced by C_d , which is of the same order of magnitude as C_{ox} and varies with the spatial distribution of the charges across the channel [2]. This renders C_g very sensitive to quantum confinement effect: As these transistors present a volume inversion regime rather than the surface electron channel of classical MOSFETs (Fig. 1), the distance between the gate and the channel is increased and the coupling reduced. In a nanoMOSFET that is small enough to present single subband occupancy, this reduction is on the order of 30%. However, as we will show here, quantum confinement can also create bumps in the $C_g(V_g)$ behavior of Silicon nanoMOSFETs due to a geometrical effect triggered each time a new subband is populated.

Fig. 2 shows the gate capacitance behavior at low and high drain voltage of a $3 \times 3 \text{ nm}^2$ cross-section gate-all-around (four gates) transistor (with a transversal effective mass of $0.19 \times m_{e0}$. Since the cross-section is square and the transversal effective mass is isotropic the second and third energy level are degenerated). These capacitance curves present variations that can be correlated to slope variations, or threshold voltages, in the I_d - V_g curves (Fig. 3). These threshold voltages are themselves related to the occupation onset of the different subbands by electrons in the channel (Fig. 4). Below threshold, the first subband is barely occupied. When V_g is increased, however, the DOS, and thus C_S , is increased. Electrons start to pile-up in the channel as well and C_d increases. As a result, C_g increases with V_g . As V_g is further increased above this first threshold, the first subband eventually becomes full, and any further increase in V_g does not result in an increase of the DOS or the electron concentration. As a result, both the current and the capacitance saturate. As the gate voltage is further increased, however, higher order subbands become populated (Fig. 4) and the current and capacitance values start to increase again. Higher order subbands not only increase the DOS and the number of electrons in the channel, but they also move the channel closer to the surface (Fig. 5) which further increases C_d and the coupling between the gate and the channel and thus C_g . This explains the increase of the slope in the I_d - V_g and the bump in the $C_g(V_g)$ curve as the charge centroid is moved towards the surface and the capacitance is increased (Fig. 6). The shape of the channel which impacts C_g depends of the number of occupied subbands *vs.* V_g . This is mainly related to the ratio of the cross-section dimensions to the effective

masses in the lateral directions. Depending of the exact channel orientation, this effect should appear in silicon for cross-section diameters ranging from about 3 to 7nm. For larger diameters, many subbands are occupied, which suppresses the quantum confinement effect and volume inversion. In smaller diameters, the energy separation between subbands is so large that in the usual V_g range only the first subband is occupied. This explains why no bump was observed in [2] for Si in a [100] $2 \times 2 \text{ nm}^2$ nanowire as confirmed also by our own 1.5×1.5 and $2 \times 2 \text{ nm}^2$ simulation results.

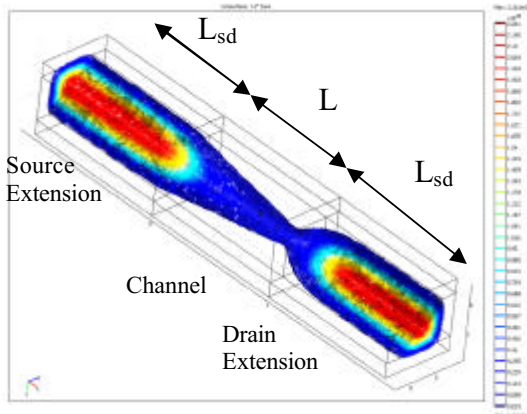


Figure 1: 3D electron concentration at threshold of a 3×3 [100] oriented GAA nanowire. $V_d=0.4V$. $L=L_{sd}=10nm$.

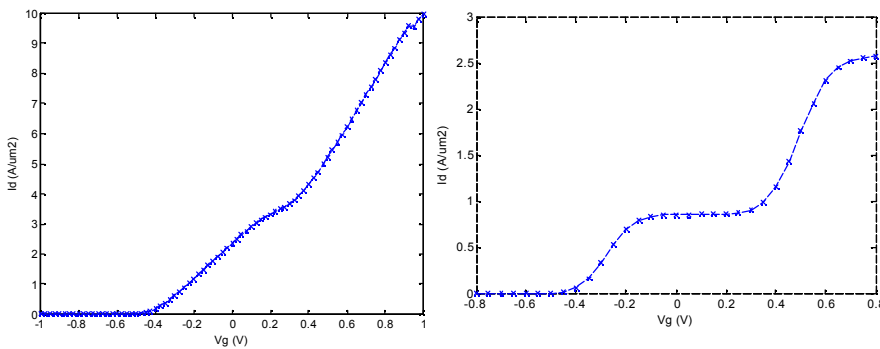


Figure 3: I_d - V_g curves at $V_d=0.4V$ (Left) and $V_d=0.1V$ (Right)

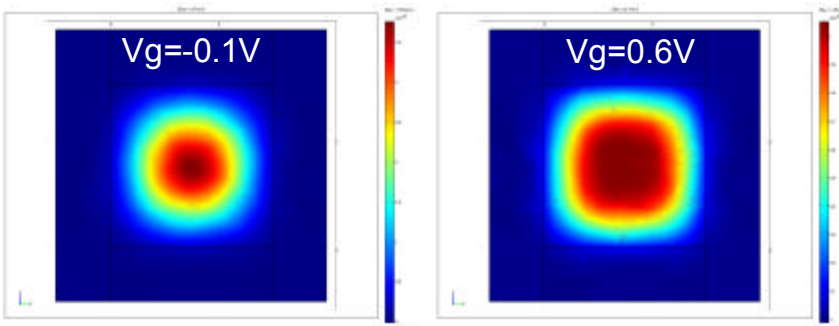


Figure 5: Electron concentration in the middle of the channel at $V_g=-0.1V$ (first subband occupied only) (left) and at $V_g=0.6V$ (first, second and third subbands occupied) (right) of the $3 \times 3 \text{ nm}^2$ cross-section Gate-all-around. As higher order subbands have their maximum occupation peak closer to the Si/SiO₂ interface, the centroid of charge move away from the center when they are occupied.

Acknowledgements

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References

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- [2] A. Marchi and Al., “Investigating the performances limits of Silicon-nanowire and carbon-nanotube FETs”, Solid-State Electronics 50, pp. 78-85, 2006.
- [3] N. Neophytou and Al., “Bandstructure Effects in Silicon Nanowire Electron Transport”, IEEE TED, Vol. 55, 2008.

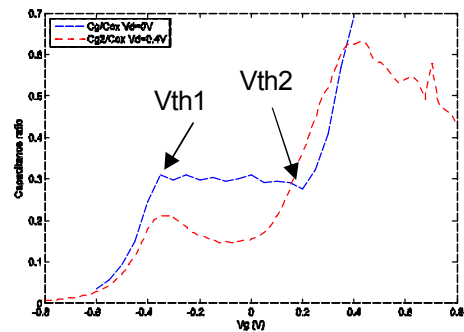


Figure 2: Gate capacitance behavior at $V_d=0$ (plain) and $0.4V$ (dashed) of a $3 \times 3 \text{ nm}^2$ cross-section Gate-all-around (four gate). $L=10nm$.

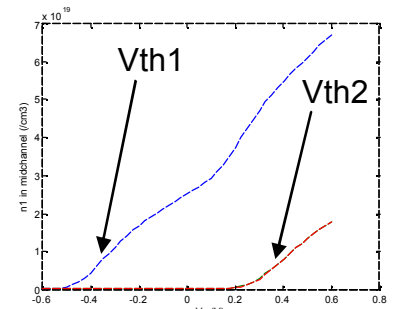


Figure 4: Occupation of the 1st (blue) and 2nd and 3rd (red) subbands in the middle of the channel by electrons vs. V_g .

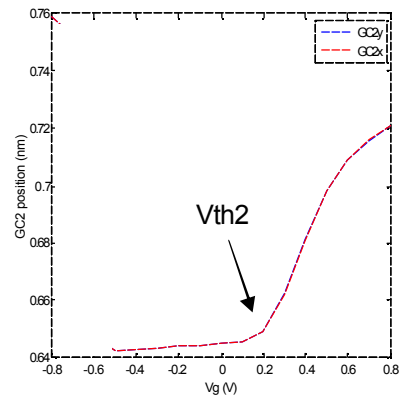


Figure 6: Average distance (centroid) of the charge from the center of the cross-section.