

Dear Colleagues,

The SOI Consortium, LETI-CEA, and Soitec are organizing an evening workshop at the Hilton Baltimore on Wednesday the 9th of December 2009 focused on FDSOI readiness.

Recent major advances in planar FDSOI devices are strongly positioning this technology towards an interception of the 22/20nm node for Low Power applications. From a design perspective, planar FDSOI is an evolutionary approach. It does not exhibit a floating body effect, thus the porting of bulk designs to FDSOI should be simple to implement. Published FDSOI CMOS work has shown that FDSOI reduces V_t variability by 50-60%, reduces I_{off} by orders of magnitude and preserves a target performance at a cost per die that is comparable or lower than the equivalent bulk. Operating FDSOI high density SRAM cells at sub-0.5V V_{dd} and in the subthreshold regime with an excellent SNM and at minimum cell size is a reality.

The goal of this workshop is to give the highest exposure to FDSOI readiness in the areas of modelling, design and EDA infrastructure. In addition to IEDM participants there will be an additional invitation list targeting industry representatives. Goal is to create a platform and expertise for fruitful exchange, discussions and understanding the potential of the fully depleted SOI architecture as a low power platform for 22nm and beyond, as well as, identifying the missing ecosystem parts that will be necessary to bring the FDSOI technology to industrial maturity and widespread adoption.

Complementing the technical papers and short courses presented during the IEDM conference, the workshop will be devoted to SRAM scaling, design porting from bulk to FDSOI, BSIM models, the results of porting an ARM core to SOI and TCAD with an outlook towards the specificities for FDSOI. The workshop provides a comprehensive review of the current state of technology presented by renowned experts in the field.

The workshop starts at 6pm and finishes at 9:15pm. In order to provide time for networking and discussions with the speakers, there will be a reception before the workshop and time for discussions and drinks at the end of the event. The program is:

| | |
|--------|--|
| 6:00pm | Reception |
| 6:40pm | Opening remarks (Dr. C. Mazure, Soitec) |
| 6:45pm | FDSOI Highlights of the IEDM 2009 (Dr. O. Faynot) |
| 7:00pm | ETSOI substrate readiness for FDSOI (Dr. B. Doris, IBM) |
| 7:15pm | Models for FDSOI: BSIM, SPICE (Prof. C. Hu, UCB) |
| 7:35pm | FDSOI Benefits for SRAM at the 22nm Node (Prof. T.J. King, UCB) |
| 7:55pm | ARM 1176 implementation in SOI 45nm technology and silicon measurement and outlook towards FDSOI (Dr. Greg Yeric, ARM) |
| 8:15pm | SOI Digital Implementation & Electrical Signoff (M. Jacobs, Cadence) |
| 8:35pm | Wrap up (H. Mendez, SOI consortium) |
| 8:40pm | Drinks, ends at 9:15 pm |

We strongly encourage you to participate in the workshop and contribute to the advancement of FDSOI technology with your questions and comments.

If you would like to attend, please send an email to: carlos.mazure@soitec.fr

We are looking forward to seeing you at the FDSOI Workshop on December 9th, at 6pm.

Horacio Mendez
Executive Director
SOI Consortium

Dr. Carlos Mazure
CTO
Soitec

Dr. Laurent Malier
CEO
LETI-CEA