FDSOI – Readiness and Manufacturability

Tomasz Brożek
PDF Solutions

FDSOI Workshop
Taipei, 28 April, 2011
Agenda

- **Introduction**

- **Device**

- **Integration**

- **Manufacturability**

- **Conclusions**

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FDSOI devices on SOI Wafers

- Krivokapic et al., IEDM 2002 (AMD)
- K. Cheng et al., VLSI 2009 (IBM)
- C. Fenouillet-Beranger et al., unpublished (ST/LETI)
- M. Fujisawa et al., IEEE SOI Conference 2005 (Toshiba)

- SOTB
- DST
- Hybrid FDSOI
- BULK

N. Sugii et al., IEDM 2008 (Hitachi)
R. Chua et al., IEDM 2001 (Intel)
C. Fenouillet-Beranger et al., IEDM 2009 (ST/LETI)

Thomas Skotnicki

IEDM 2010 Short Course - CMOS Technologies – Trends, Scalability and Issues
Introduction

- Assess readiness and manufacturability of proposed solutions
- Identify potential barriers and roadblocks which need addressing
- Use public sources of information about FDSOI device, process, and technology
  - Avoid comparison between different device contenders, and avoid "endorsements"

- Proposed Scorecard table – to be discussed and filled at the end of the Workshop

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Readiness</th>
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<tbody>
<tr>
<td>Device Performance</td>
<td></td>
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<tr>
<td>Device Variability</td>
<td></td>
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<tr>
<td>Scalability and Extendibility</td>
<td></td>
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<tr>
<td>Integration</td>
<td></td>
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<tr>
<td>SoC Platform – Completeness</td>
<td></td>
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<tr>
<td>Design PDK, Modeling environment</td>
<td></td>
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<tr>
<td>Reliability/Robustness</td>
<td></td>
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<tr>
<td>Cost (substrate and final wafer cost)</td>
<td></td>
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<tr>
<td>Manufacturability</td>
<td></td>
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<tr>
<td>Compatibility with Existing Process</td>
<td></td>
</tr>
<tr>
<td>Readiness and Maturity</td>
<td></td>
</tr>
<tr>
<td>Process Control</td>
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<tr>
<td>Yield</td>
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</table>
Device Performance

- DC Device performance adequate for Low Power and General Purpose requirements
- Very good electrostatics, Low DIBL, suppression of SCE
- Vmin reduction potential due to excellent SS and low local variability

**Representative Device Characteristics**

- \( L_G = 25 \text{ nm} \)
- \( V_{DS} = 0.9 \text{ V} \)
- \( T_{inv} = 1.6 \text{ nm} \)

<table>
<thead>
<tr>
<th></th>
<th>NFET</th>
<th>PFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS (mV/dec)</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>75</td>
<td>95</td>
</tr>
<tr>
<td>loff (pA/\mu m)</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>GIDL (pA/\mu m)</td>
<td>15</td>
<td>5</td>
</tr>
<tr>
<td>Ion (\mu A/\mu m)</td>
<td>640</td>
<td>490</td>
</tr>
</tbody>
</table>

- Excellent subthreshold swing (SS = 80 mV/dec)
- Superior short-channel control (DIBL< 100mV/V)

**FDSOI is a serious candidate for next generation LP/G technology**

**UTB SOI substrates with very good thickness control needed to move forward**

K. Cheng et al. – IBM/ST – IEDM’2009

V. Barral et al., IEDM’07
Device Variability

- Very good device matching demonstrated by LETI, ST, and IBM
- RDF suppressed by use of undoped Si
- \( V_t \sim T_{Si} \) dependence through SCE
- Very good \( T_{Si} \) control and low variability
  - Need more data on random, short range, and long range variation components

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Undoped substrate helps to achieve low variability and enables Vdd reduction
Need further verification of matching for smaller \( L \) and \( W \) (down to ~ 10nm)
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**Figure 2** Pelgrum plots of 8.5nm \( T_{Si} \) FDSOI nMOSFETs. \( \sigma_{Vt} \) differences between \( V_g=50\text{mV} \) and \( V_g=1\text{V} \) for \( L=25\text{nm} \) allow us to evaluate \( \sigma_{Vt} \) by using the inserted equation and experimental values of \( dV_t/dL \) and \( dV_t/dT_{Si} \) (Fig.3).

**Figure 3** \( V_t(L) \) and \( V_t(T_{Si}) \) with the respective derivatives. The difference between \( dV_t/dT_{Si} \) at 50mV and 1V is weak and thus the term which includes \( \sigma_{Vt} \) in \( \sigma_{Vt,L} \) in Fig.2 can be neglected, especially at \( T_{Si}=8.5\text{nm} \).
Scalability

- Full benefits of FDSOI is based on reduced variability and very good electrostatics
- Need thin Si and UTBOX ($L_{gate}/T_{si} > 3$, for thick BOX, but can be relaxed with UTBOX)
  - Trends are that for $L_{gate} \approx 40 \text{ nm} \rightarrow T_{si} \approx 8 \text{ nm}; L_{gate} \approx 30 \text{ nm} \rightarrow 6 \text{ nm}$
  - By thinning BOX, FDSOI believed to be scalable to $L_g \approx 10 \text{ nm}$ with $T_{si} \approx 7 \text{ nm}$
- Gate scaling and Gate integration choices same as for Bulk and PDSOI

- Silicon Thickness and BOX Thickness essential for SCE control
- FDSOI with UTBOX requires Ground Plane and related processing steps
- Further Si thickness reduction will have larger impact on $R_{sd}$ resistance
- BOX thinning with GP will have negative impact on parasitic capacitance
Consequences of Thin SOI and UTBOX – Bill to pay

- Thin SOI and UltraThin BOX are both enablers of FDSOI CMOS platform, they are also root causes of some of the problems

<table>
<thead>
<tr>
<th>Issue</th>
<th>Reason</th>
<th>Impact</th>
<th>Known Solution</th>
<th>Trade-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Rext</td>
<td>Thin Si layer Underlapped junction</td>
<td>DC and AC performance</td>
<td>S/D extension doping</td>
<td>Channel doping &quot;contamination&quot; esp in short Lg (~ 10nm); RDF</td>
</tr>
<tr>
<td>High Cov</td>
<td>Thin BOX</td>
<td>AC performance, Dynamic Power</td>
<td>Localized self-aligned GP under channel only</td>
<td>Process control, complexity</td>
</tr>
<tr>
<td>Mobility</td>
<td>Thin Si layer</td>
<td>Increased scattering</td>
<td>Improve interfaces!</td>
<td>unknown</td>
</tr>
<tr>
<td>Through channel shallow implant</td>
<td>Thin BOX GP implants</td>
<td>Possible &quot;sprinkle&quot; channel doping; RDF</td>
<td>???</td>
<td>unknown</td>
</tr>
<tr>
<td>Reduced emb. S/D strain</td>
<td>Thin Si layer</td>
<td>Less mobility enhancement</td>
<td>- Shallow recess</td>
<td>- Risk of complete etch</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Faceted RSD</td>
<td>- Pitch/density effect</td>
</tr>
<tr>
<td>Self-heating</td>
<td>Thin Si on BOX</td>
<td>Poor Heat conduction through BOX</td>
<td>Forced cooling</td>
<td>Added cost and complexity</td>
</tr>
<tr>
<td>Narrow Process Window</td>
<td>Thin Si Thin BOX</td>
<td>Yield loss Variability</td>
<td>High selectivity process</td>
<td>Development cost and complexity</td>
</tr>
</tbody>
</table>

- With further reduction of Tsi and BOX thickness, thickness variability will contribute more to overall device variability
- None of the issues above seem to be a show-stopper for FDSOI use at 20nm node
Integration

- Promising simplicity
  - Simplified Front End of Line – reduced number of litho steps
  - MOL and BEOL same as other options

- Ground Plane integration and Multi-Vt devices will complicate process flow

Table 1 Advantages of the new ETSOI CMOS flow.

<table>
<thead>
<tr>
<th></th>
<th>Bulk CMOS</th>
<th>New ETSOI CMOS flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device formation</td>
<td>Implant</td>
<td>Implant-free</td>
</tr>
<tr>
<td>Isolation</td>
<td>Challenging</td>
<td>Simple</td>
</tr>
<tr>
<td>Well implant</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Halo</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Random dopant fluctuation</td>
<td>Severe</td>
<td>Minimal</td>
</tr>
<tr>
<td># Mask levels to form S/D</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>HK/MG stack</td>
<td>2 band-edge</td>
<td>1 mid-gap</td>
</tr>
<tr>
<td>Resist shadowing</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Gate-height scaling</td>
<td>Difficult</td>
<td>Easy</td>
</tr>
<tr>
<td>(dopant punchthrough)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant damage</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>ETSOI amorphization</td>
<td>N/A</td>
<td>No</td>
</tr>
<tr>
<td>Resist strip</td>
<td>Challenging</td>
<td>Easy</td>
</tr>
</tbody>
</table>

K. Cheng et al. – IBM/ST – IEDM’2009

- Device Build can be simplified because of the "pre-work" done at the substrate level
- SOC platform requires more complete integration, which can bring other issues
Integration Compatibility

- Significant work done on FDSOI integration
- R&D Labs continue working on device optimization, process integration, and optimal design environment
- Important to early identify roadblocks and process culprits to avoid pursuing wrong solutions
- Detailed characterization needed to explore module interactions, process capability, and design tolerances

### Process integration comparison

<table>
<thead>
<tr>
<th>Process step</th>
<th>bulk</th>
<th>Planar FDSOI</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si thinning ($T_{Si}$)</td>
<td>no</td>
<td>variability: $SCE_{(Tsl)}$</td>
<td>variability: $W_{eff}(Tsl)$, topography vs. density</td>
</tr>
<tr>
<td>Well &amp; $V_T$ doping (N)</td>
<td>variability, mobility</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>Isolation (W)</td>
<td>STI process, latch-up</td>
<td>mesa or thin STI</td>
<td>mesa, variability: $SCE_{(W)}$</td>
</tr>
<tr>
<td>Metal gate $W_f$</td>
<td>dual band edge</td>
<td>single mid-gap for LP, $V_T$ adjustment.</td>
<td></td>
</tr>
<tr>
<td>S/D implantation</td>
<td>$R_{acc}$ vs. $SCE$</td>
<td>Amorphisation $R_{acc}$</td>
<td>amorphisation, 3D doping ($R_{acc}$)</td>
</tr>
<tr>
<td>S/D epitaxy</td>
<td>SiGe for strain</td>
<td>down to 2.5nm</td>
<td>dewetting</td>
</tr>
<tr>
<td>Strain &amp; mobility boosters</td>
<td>CESL, SMT, eSiGe</td>
<td>CESL, sSOI, SiGe</td>
<td>CESL, eSiGe</td>
</tr>
</tbody>
</table>

F. Andrieu (LETI) – EuroSOI’2008

- Overall FEOL integration aligned with "typical" process (Bulk or SOI), but many specific operations required process development
- Although many of them passed "prove of concept", still require full integration validation
Compatibility with Existing Integration - Comments

- **Isolation**
  - Shallow STI vs Mesa isolation
  - Risk of epi growth on substrate if edge exposed

- **Source/Drain Region**
  - Reduced opportunity for recess (up to 4-5nm?)
    - Risk of full removal of "seed" layer for epi
      - Requires very good etch uniformity control through pitch, across layout patterns (as well as across wafer, wafer-wafer)
      - Agglomeration or surface "wetting" problems of thin seed
  - In-situ highly doped e-SiGe and e-SiC/Si raised junctions
    - eSiGe etchback vs epi block layers
      - eSiGe etchback requires very high selectivity to Si
  - Junction extensions doping
    - Tilted Implant? Amorphization?
      - Is amorphization compatible with eSiGe and eSiC?
    - Unimplanted? Controlled by Epi dopant concentration and anneal?

- **Gate integration**
  - HK-MG with Gate Last process is a dominating trend for 20 nm
  - Similar impact and consequences as for Bulk
  - However, RMG limits options for "Hybrid" FDSOI/Bulk integration
### Compatibility with Gate Integration Solutions

#### Note – Gate Last integration is a dominating gate integration choice for 20nm LP
- There are probably serious reasons for Gate Last being chosen above Gate First
- Gate Last is a proven solution in manufacturing for 2 generations

#### Most of FDSOI data is from Gate First
- No obvious barriers to integrate with Gate Last, but need experimental confirmation and data

<table>
<thead>
<tr>
<th>FDSOI</th>
<th>Gate scalability</th>
<th>Gate Stack</th>
<th>Mobility boosters</th>
<th>HV devices – Dual Gate</th>
<th>Silicide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate First</td>
<td>Same as BULK/SOI</td>
<td>Thermal Budget?</td>
<td>Weakened</td>
<td>&quot;Hybrid&quot; FDSOI/Bulk I/O HV devices with deposited oxide (cannot afford thick oxidation)</td>
<td>Same issues as BULK/SOI</td>
</tr>
<tr>
<td></td>
<td>Possibly two generations</td>
<td>May be more difficult to set Vt with gate Stack only</td>
<td>- Raised epi S/D</td>
<td></td>
<td>NiSi growth on SiGe and SiC</td>
</tr>
<tr>
<td>Gate Last (RMG)</td>
<td>Same as BULK/SOI</td>
<td>May be more difficult to set Vt with gate Stack only</td>
<td>Weakened</td>
<td>Cannot do &quot;Hybrid&quot; I/O HV devices with deposited oxide</td>
<td>Same issues as BULK/SOI</td>
</tr>
<tr>
<td></td>
<td>Replacement Gate limitations?</td>
<td></td>
<td>- Raised epi S/D</td>
<td></td>
<td>NiSi growth on SiGe and SiC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Metal Gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Strained substrate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

"Note – Gate Last integration is a dominating gate integration choice for 20nm LP
- There are probably serious reasons for Gate Last being chosen above Gate First
- Gate Last is a proven solution in manufacturing for 2 generations

Most of FDSOI data is from Gate First
- No obvious barriers to integrate with Gate Last, but need experimental confirmation and data
Re-usability of Strain solutions in FDSOI

FDSOI has very limited choices for mobility enhancement with process-induced stress.

<table>
<thead>
<tr>
<th>Strain Sources</th>
<th>BULK Gate First</th>
<th>BULK Gate Last</th>
<th>Planar FDSOI Gate First</th>
<th>Planar FDSOI Gate Last</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stressed Liner (t-CESLc-CESL)</td>
<td>Limited</td>
<td>Raised S/D Trench Cnt</td>
<td>Limited and reduced by Raised S/D Trench Cnt</td>
<td></td>
</tr>
<tr>
<td>SMT - GATE</td>
<td>Reduced by MG</td>
<td>No PolySi</td>
<td>Reduced by MG</td>
<td>No PolySi</td>
</tr>
<tr>
<td>SMT – S/D</td>
<td>Possible</td>
<td>Possible</td>
<td>Not Possible</td>
<td>Not Possible</td>
</tr>
<tr>
<td>embSiGe</td>
<td>With Recess</td>
<td>With Recess</td>
<td>Raised S/D Faceted</td>
<td>Raised S/D Faceted</td>
</tr>
<tr>
<td>Contact Stress (LI)</td>
<td>Limited Cnt Vol</td>
<td>Limited Cnt Vol</td>
<td>Raised S/D</td>
<td>Raised S/D</td>
</tr>
<tr>
<td>Replacement Gate Stress Enhancement</td>
<td>No</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal Gate material</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Strained Substrate</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

- Reduced use of "traditional" mobility boosters limits device performance
- However, this also reduces their contribution to device variability

Based on 28/32nm projected to 20nm

Strain transfer to thin channel from raised source/drain SiGe. Uniaxial strain in the channel is about 0.3% (>1% achieved in Bulk).

Intel 45nm – K. Mistry et al., – IEDM’2007
Intel 32nm – P. Packan et al., – IEDM’2009
Intel 32nm – Natarajan et al., – IEDM’2009

A. Khakifirooz et al. - IBM – 2010

Intel 32nm – K. Mistry et al., – IEDM’2007
Intel 45nm – K. Mistry et al., – IEDM’2007
Intel 32nm – P. Packan et al., – IEDM’2009

PMOS
NMOS
Poly Si
Remove Pol Si
Deposit Metal Gate
FDSOI GATE
Reduced Cnt Vol
Strain transfer to thin channel from raised source/drain SiGe. Uniaxial strain in the channel is about 0.3% (>1% achieved in Bulk).
## SoC Platform Readiness

<table>
<thead>
<tr>
<th>Component</th>
<th>Possible</th>
<th>Integration</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi Vt devices</td>
<td>Yes</td>
<td>Dual WF Metal Gate</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BackPlane back bias</td>
<td></td>
</tr>
<tr>
<td>SRAM</td>
<td>Yes</td>
<td>With GP</td>
<td>None</td>
</tr>
<tr>
<td>I/O HV transistors</td>
<td>Yes</td>
<td>Dual Gate dielectric (deposited) or through Hybrid Bulk integration</td>
<td>May be difficult to integrate using Gate Last (Planarity) – it may also not support long Lgate</td>
</tr>
<tr>
<td>Passives (resistors, capacitors)</td>
<td>Yes</td>
<td>Thin Film Resistors, FET capacitors/varactors BEOL MIM capacitors</td>
<td>None</td>
</tr>
<tr>
<td>rf, Analog</td>
<td>Yes</td>
<td>Analog - HV devices</td>
<td>As I/O HV transistors</td>
</tr>
<tr>
<td>ESD protection</td>
<td>Yes</td>
<td>Through Hybrid Bulk integration or using Trbased ESD scheme</td>
<td>Process complexity</td>
</tr>
<tr>
<td>Power devices (LDMOS, etc)</td>
<td>Yes</td>
<td>Hybrid Bulk Integration</td>
<td>Process cost and complexity</td>
</tr>
<tr>
<td>Bipolar transistors</td>
<td>Yes</td>
<td>Hybrid Bulk Integration</td>
<td>Process cost and complexity</td>
</tr>
</tbody>
</table>

- **Full SoC platform offering may require co-integration with Bulk**
- **What are process complexity and manufacturability consequences?**
SoC platform – Multi Vt Devices

Multi-Vt devices can be achieved in FDSOI in several ways (without additional channel implant)

- Combination of dual Metal Gate and Dual-Doped Ground Plane looks most promising
- Applying Back Plane Bias allows additional Vt adjustment

O. Weber et al. – LETI/STM/Soitec – IEDM’2010

O. Faynot et al., – CEA-LETI – IEDM’2010

Fig. 3: Effective work-function (EWF) vs EOT for the gate stacks of this study compared to general trends in high-k/metal gate stacks.

Fig. 14: Possible solutions to achieve a large range of \( V_T \)'s with FDSOI technology

Fig. 15: Experimental \( V_T \)'s achieved for \( nMOS \) and \( pMOS \), depending on the chosen metallic layer
SoC – HV devices for I/O

- **I/O and HV device integration**
- **Dual Gate Dielectric – Thick + Thin Oxide**
  - Similar integration as in Bulk
  - Need deposited oxide to reduce Tsi loss
- **Hybrid "FDSOI + Bulk" integration of HV devices and ESD protection**
  - May not be RMG compatible

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**Very narrow POP CMP and Poly Etch Process window:**
Step Height difference of ~ 20nm, with Poly Gate height ~ 40 – 50 nm

- **No barrier for building Dual Gate Dielectric Thickness** (need high quality oxide)
- **Hybrid FDSOI + Bulk integration not compatible with Replacement Metal Gate**
Manufacturability – Process Control

- **Paradigm shift in Wafer manufacturing**
  - Si substrate becomes part of the Device solution
    - This part of the process is outside of the IC manufacturer control
    - Incoming wafer control will need much broader and stringent specification
    - Shared responsibility for substrate control
      - Quality control and certification on substrate manufacturer side
      - Incoming material control on the wafer Fab side

- **Incoming wafer quality control**
  - Physical dimensions and specs
    - SOI thickness
    - BOX thickness
    - Wafer flatness
    - Surface roughness
    - Stress (if applicable)
  - Process control for defectivity
    - Doping variation
    - Contamination
    - SOI defects
    - BOX defects/pinholes

- **Wafer Control during processing**
  - SOI silicon loss
  - Process induced damage
  - Stress relaxation
Manufacturability - Ground Plane Integration

- **High Dose Ion Implantation through SOI**
  - Risk of implant tail in thin Si layer
    - Adding to substrate doping and variability
    - How to reduce the straggle and risk of channel doping?
  - Risk of damaging the Si layer
    - Partial amorphization
    - Interaction with other defects already present in thin Si
  - Risk of damaging thin BOX layer
    - BOX now has to have good integrity (Gate oxide grade)
    - High quality interfaces required

- **Post Implantation anneal for damage repair**
  - Compatibility with Strained SOI substrate?
  - Defect gettering at BOX interfaces – impact on BOX integrity?

- **Process control and metrology**
  - Electrical characterization required for evaluation of the above issues
  - Process optimization requires high observability and fast cycle time

- Ground Plane integration may inadvertently impact SOI properties and defectivity
- Complete integrated solution for SoC needs full electrical characterization
Manufacturability – Process Control

- Consequences of thin Si on Thin BOX
- Two areas of special concern
  - Physical interaction with thin SOI layer
    - Si loss (Oxidation, Etch, CMP...)
    - Control of Si thickness – impact on device performance and variability
    - Need of seed layer for epi Source/Drain
    - BOX punchthrough due to mechanical damage (Etch and CMP)
    - More sensitive than Bulk → Shorts to the substrate
  - Sensitivity to Plasma-Induced Charging
    - BOX integrity needs to be preserved till end of processing
    - Although Antenna Ratio for Process induced charging is very small (< 1) total area of the oxide under stress is very large
    - Defects and weak BOX spots may break down under Process-induced charging

"Traditional" Antenna-Enhanced Charging
- large charging area
- small gate dielectric area → large AR
- damage due to "intrinsic wear-out"
- trap/charge generation in oxide
- in worst case – breakdown
- Breakdown voltage - high

FDSOI - specific Charging damage at "weak spots"
- large charging area
- large gate dielectric area → small AR
- damage due to "weak spot" rupture
- localized current concentration
- in worst case – breakdown
- Breakdown voltage - low

Antenna

Gate

F-N tunneling

Si-substrate

oxide defect

"Traditional" Antenna-Enhanced Charging

F-N tunneling
UTTB Specific Processing Requirements

- UTBB may have impact on some of the process steps
- New tools or process recipes may become available to enable better process

<table>
<thead>
<tr>
<th>Process steps</th>
<th>Characteristics</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>STI CMP</td>
<td>CMP of ultra-shallow STI with low topology</td>
<td>Highly selective, low defectivity CMP process (can relax planarization needs)</td>
</tr>
<tr>
<td>Poly and Spacer Etch</td>
<td>No Si substrate loss</td>
<td>High selectivity soft landing</td>
</tr>
<tr>
<td>Epi Raised S/D</td>
<td>Low resistance, consistent stress</td>
<td>Highly uniform process with minimum loading, very well controlled variability</td>
</tr>
<tr>
<td>Contact or Trench Contact Etch</td>
<td>Cannot short to substrate</td>
<td>Controlled, selective Etch Stopping above substrate</td>
</tr>
<tr>
<td>Implant and plasma processing (Etch, PECVD, PVD)</td>
<td>No process induced charging damage</td>
<td>Uniform plasma and process steps optimized for low charging</td>
</tr>
</tbody>
</table>

- Process development may be needed to optimize specific unitary steps
- Charging properties can be studied with wafer based sensors (CHARM-2, KLA), but "charging process window" needs to be correlated to real device sensitivities
- Tool FDC trace analysis and monitoring may help to reduce charging
Design Rules and DFM

Design rule set-up similar to Bulk process, with some "extras"
- Ground Plane and Substrate contact DR
- Active and Isolation DR's need to account for lateral Epi overgrowth
- Some DR's simplified or not needed; e.g., Well Proximity

Un-landed contacts not supported?
- Risk of Contact Short to substrate higher than in Bulk
- Is there a density penalty related to Contact enclosure?

Layout attribute dependence of device performance
- Poly Pitch and Active Extension length and width
  - Epi growth sensitivity → Stress, resistivity
  - Active Proximity (in-line and perpendicular) – stress distribution, cross Gate diffusion

Restricted, regular design will reduce possible process risks and sensitivities

- Active, Isolation, and Junction integration may require special DR (and validation)
- Device sensitivity to layout attributes need to be characterized in detail to support all models and design kits
- Regular template based layout design reduce variability and simplify characterization
Technology characterization needs

- Both FDSOI devices and integration scheme has been demonstrated in R&D lines
- Significant experience and lessons learned allow compilation of known process risks, failure modes, marginalities, and sensitivities
- FDSOI for LP SoC platform requires in depth assessment of ETSOI/UTBOX integration specific DR's, systematics, and Process Window characterization
- Combination of electrical testable structures, metrology, defectivity, and PFA is needed for process characterization and fast paced development

Example of Contact Process Window Characterization for Yield – PDF internal

40nm design rule 54x54 structures fail more than nominal 60x60 structures
40nm Shared Cnt performance is worse than 45nm for same overlap
40nm CA-to-PC shorts performance is worse than 45nm
Device Layout Sensitivities and Silicon Validation

Characterization Experience - Accurate and comprehensive characterization will be essential for effective utilization of either of the technology choices for SoC designs.

Layout Effects in Nanometer Technologies

- Printability and stress effects increase systematic layout variation

<table>
<thead>
<tr>
<th>Systematic variation (±)</th>
<th>Root causes</th>
<th>Impact at the 45/32nm technology node</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate poly orientation</td>
<td>Poly lithography</td>
<td>N/A</td>
</tr>
<tr>
<td>Gate poly pitches</td>
<td>Poly OPC and lithography</td>
<td>3-5% - printability</td>
</tr>
<tr>
<td></td>
<td>Stress Layers</td>
<td>15% - poly pitch related stress</td>
</tr>
<tr>
<td></td>
<td>Loading effects from Etch and film deposition</td>
<td>5% - contact space related stress</td>
</tr>
<tr>
<td>Poly corner rounding</td>
<td>Poly OPC and lithography</td>
<td>15%</td>
</tr>
<tr>
<td>Transistor location in multi-gate transistor</td>
<td>Poly patterning and stress impacted by local neighborhood differences</td>
<td>15%</td>
</tr>
<tr>
<td>Active corner rounding</td>
<td>OPC and lithography, stress</td>
<td>7%</td>
</tr>
<tr>
<td>Un-modeled narrow width effects</td>
<td>Stress effects, poly step height</td>
<td></td>
</tr>
<tr>
<td>Gate to active edge</td>
<td>STI stress, e-SiGe stress</td>
<td>10-20% for PMOS with e-SiGe</td>
</tr>
<tr>
<td>Well proximity</td>
<td>Implant scattering</td>
<td></td>
</tr>
<tr>
<td>Nwell-Pwell separation</td>
<td>Gate counterdoping and misalignment</td>
<td></td>
</tr>
<tr>
<td>Contact density and placement</td>
<td>Silicide sheet resistance and stress layers</td>
<td></td>
</tr>
</tbody>
</table>

45nm NMOS Idr Shift vs. Layout

<table>
<thead>
<tr>
<th>45nm PMOS Idr Shift vs. Layout</th>
<th>Process 1</th>
<th>Process 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA extension</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Poly Necking</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Pitch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AA flaring</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact density &amp; placement</td>
<td></td>
<td></td>
</tr>
<tr>
<td>device location</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Device Variability Reduction for Regular Layout

30-35% reduction in $I_{dsat}$ variability for the template-based patterns vs. Restricted Design Rule (RDR) layout for bulk CMOS 28nm technology

Comprehensive Characterization environment allows high-resolution assessment of layout effects and other systematics
Summary

- FDSOI technology seems to be a viable contender for LP & GP technologies but to succeed, it cannot be a single node solution
  - It's crucial to establish UTBB for 20nm node at a leading foundry
  - New process integration and interaction with devices – not fully characterized
  - Dependence on incoming substrate quality

- Increased role and responsibility of substrate manufacturer
  - UTBB provided by substrate supplier
  - Move in the supply chain with more value added from substrate vendor
  - Wafer quality control needed on both side of the divider

- SOC readiness (and cost)
  - Concept prove-outs done
  - Basic components and design environment still under development
  - Need to lock the technology integration choices
  - Need focused efforts for process characterization and qualification, DR validation, and model closure
  - Si-based PDK and roadmap needed by 1H 2012