SOI CMOS Technology Through 7nm

Rama Divakaruni, IBM
Outline

- Introduction: Technology Migration and Challenges
- 14nm Choices and Results
- 10nm Directions
- 7nm Challenges
- Summary
Major technology innovations “saturate” after about a decade
“Disruptive” Innovations will enable the next decades of progress
Design and Technology Co-Optimization key to coming Innovations
SOI Value Adders

• Superior Isolation
  – No Well Taps required
  – Smaller circuit foot-print
  – Latch-up free operation

• High Speed Switching
  – 2X lower junction perimeter capacitance
  – Improved Short-Channel Effects

• Less susceptibility to soft errors
  – SER reduced by 5-7X
  – Low power high reliability

• Reduced Variation within Die
  – Short-channel Vt roll-off suppression
  – Less variation in Vt vs Lgate.
  – No Well-Proximity Effects (no deep wells in SOI)
SOI Enabled Device Structure Pipeline

Scaling beyond 22nm requires alternative device structures

- **Fully Depleted Devices**
  - ETSOI/UTBB
  - Si Nano-Wire

- **Conventional Planar Device**
  - FinFET

- **22/20 nm**
  - 14/10 nm
  - 7 nm & Beyond

EFK
Albany Nanotech
Yorktown Research
Ten Generations of IBM SOI Technology

Sustained innovation in IBM technology

130/180 nm Gen 1&2 H/S PDSOI
65 nm Advanced Strained Silicon (DSL + SOI e-SiGe)
45 nm SOI eDRAM + Immersion litho + Ultra Low-k metal dielectrics
32 nm High-K gate dielectric on SOI + SOI eDRAM with Hi-K trench
22 nm 2nd Gen. HiK Gate + SOI Hi-K eDRAM w/ Epi Plate
14nm SOI FinFET with 3rd Gen.HiK + Hi-K e-DRAM with FIN
10nm 2nd Gen. FinFET + SAC + SIT BEOL
7 nm EUV + 3rd Gen. FINFET

Generations of Technology Leadership
SOI Enabled Integration : DRAM & Logic

Innovations to Obtain High Performance Systems

• Technology:
  ➢ Use SOI buried oxide to simplify process & reduce parasitics
  ➢ Scale the pass transistor for higher performance

• Design:
  ➢ Address retention through concurrent refresh
  ➢ Innovative direct sense architecture for performance
How SOI Facilitates eDRAM

Process Simplification: ~10-15% Adder

Collar process elimination

- Bulk
  - M1 Bitline
  - CA
  - WL
  - N
  - P
  - N
  - P-WELL
  - N-Band
  - Vertical Parasitic Device
  - P- Handle
  - Thick Oxide Collar to shutoff parasitic
  - Buried Plate

- SOI
  - M1 Bitline
  - CA
  - WL
  - N
  - P
  - N
  - Buried Oxide (BOX)
  - No Vertical Parasitic Device
  - No Collar Required

Buried Plate process elimination

- Epi Handle SOI
  - M1 Bitline
  - CA
  - WL
  - N
  - P
  - N
  - Buried Oxide (BOX)
  - N+ epi / P- Handle
  - Plate is now Built into SOI wafer

Integrated Embedded Memory Solutions

- Memory is 50-70% of the die – key to optimizing performance
- High Performance eDRAM delivers 3X more memory at same die size & power
  - 3X density benefit vs SRAM
  - > 5X standby power benefit
  - > 1000X SER benefit
- Compact decoupling cap for noise reduction and I/O is a great bonus!

Power 7+ Process Chip
- 567mm² 32nm SOI eDRAM technology
- Eight processor cores
- 80MB on chip eDRAM shared L3
- Equivalent function of 5.4B transistors due to eDRAM efficiency

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SOI From Fundamental Research to Product!

From research breakthroughs to real-world solutions...

- **Fundamental Research**
  - Screen new materials & processes
  - Patterning solutions
  - High-k / metal gate
  - Device structures
  - Stress techniques
  - Interconnects
  - Ultra low-k
  - Packaging
  - IBM Almaden, Zurich & Yorktown

- **Advanced Semiconductor R&D**
  - Innovation in integrated device & process technology
  - Equipment
    - Partners disclosed under NDA
  - Research
    - Partners disclosed under NDA
  - Albany Nanotech Center

- **Technology Development**
  - Multi-company co-located joint development
  - High perf SOI
    - Partners disclosed under NDA
  - Foundry bulk
    - Partners disclosed under NDA
  - IBM East Fishkill

- **Worldwide Manufacturing**
  - Process synchronized fabricators (GDSII compatible)
  - High perf SOI
    - IBM & GLOBALFOUNDRIES
  - Foundry bulk
    - IBM, Samsung, UMC, STMicro & GLOBALFOUNDRIES
  - USA, Korea, Singapore, Taiwan, Germany
CMOS Beyond 14nm: Key Challenges

- Device
- Patterning
- Interconnect
- Pipeline of innovation/collaboration
Double Patterning Solutions for Sub-80 nm

**Sidewall Image Transfer (SIT)**
- Amenable for Lines / Spaces
- Exploits “self-alignment” via anisotropic “spacer” etch

**Litho-Etch-Litho-Etch (LELE/PS)**
- Amenable for Trenches / Holes
- Employs bright field imaging (w/ NTD) for larger process window

**Self-Aligned Vias (SAV)**
- Uses trough-first-metal hardmask integration to ensure via to metal contact
- Metal and/or via can be single or double patterned

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12 October 14th, 2013 Shanghai, China
Silicon on Insulator Technology Summit
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### Patterning Overview

<table>
<thead>
<tr>
<th></th>
<th>20nm</th>
<th>14nm</th>
<th>10nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion (RX)</td>
<td>SE + Cut</td>
<td>SIT + Block</td>
<td>SIT + 2-color cut</td>
</tr>
<tr>
<td>Poly (PC)</td>
<td>SE + Cut</td>
<td>SE + Cut</td>
<td>SIT + Cut</td>
</tr>
<tr>
<td>Trench Silicide (TS)</td>
<td>SE + Cut</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Diffusion Contact (CA)</td>
<td>SE</td>
<td>PS</td>
<td>PS (SAC)</td>
</tr>
<tr>
<td>Poly Contact (CB)</td>
<td>SE</td>
<td>PS</td>
<td>PS</td>
</tr>
<tr>
<td>1&lt;sup&gt;st&lt;/sup&gt; Via (V0)</td>
<td>PS (SAV)</td>
<td>PS (SAV)</td>
<td>PS (SAV)</td>
</tr>
<tr>
<td>1&lt;sup&gt;st&lt;/sup&gt; Metal (M1)</td>
<td>PS/SE</td>
<td>PS</td>
<td>3-color PS</td>
</tr>
<tr>
<td>1x Vias (Vx)</td>
<td>SE (SAV)</td>
<td>SE (SAV)</td>
<td>PS (SAV)</td>
</tr>
<tr>
<td>1x Metals (Mx)</td>
<td>PS</td>
<td>PS</td>
<td>SIT</td>
</tr>
<tr>
<td>Critical Mask Count (RX→ M3)</td>
<td>18</td>
<td>19</td>
<td>23/24</td>
</tr>
</tbody>
</table>

**SE** = single expose  
**DP** = double patterning  
**PS** = pitch split  
**SIT** = sidewall image transfer

**NET**: 7nm will be EUV? (Triple Patterning cost/complexity!)
BEOL Interconnect Scaling Challenges

<table>
<thead>
<tr>
<th>Performance (R &amp; C)</th>
<th>Metal Reliability (Electromigration)</th>
<th>Insulator Reliability (TDDB)</th>
</tr>
</thead>
</table>

- **Cu Resistivity**: 32 nm node ρ=3.9 µΩcm, 65 nm node ρ=2.3 µΩcm, 45 nm node ρ=3.0 µΩcm

- **Cu Wire Lifetime**: Nanoscale patterning can lead to defective Cu metallization, which is fatal for EM

- **Dielectric Constant**:
  - 2.2
  - 2.4
  - 2.55
  - 2.75

  *Huge risk for very small gain*

- **Cohesive Strength, Γ (J/m²)**:

  - Nominal Dielectric Constant, k
    - 1.0
    - 1.5
    - 2.0
    - 2.5
    - 3.0
    - 3.5
    - 4.0
    - 4.5
    - 5.0

  - Increased TDDB fail rate

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Many *intrinsic* advantages in FinFET

- **Enhanced control of Short Channel Effect (SEC)**
  - Multiple gates control the channel SCE in FF
  - Doping controls the SCE in bulk

- **Significant DIBL reduction**
  - With fully-depleted device capability
  - Better electrostatics

- **Excellent low Vdd performance**
  - Performance roll-off with Vdd not as significant as bulk
  - Potential for lower power operation

- **Scalability for many generations once isolation is fixed**
Electrical vs. Physical FET Width “Fin-Effect”

- FinFETs can be electrically ‘wider’ than their physical foot-print
- Electrical $W_{\text{EFF}} \sim 1 \text{ to } 2 \times W_{\text{Physical}}$ possible.
- FET Specifications quoted per $W_{\text{EFF}}$
- Physical Densities (current and power) can be up to 2X higher (C and I)

**Example:** Consider 2 Finfets

Fin Pitch = 50nm
Hfin = 40nm
Dfin = 15nm

$W_{\text{EFF}} = 2 \times (2 \times 40\text{nm} + 15\text{nm}) = 185\text{nm}$

Physical foot print = 100nm
Current FinFETs: Bulk Isolated vs Oxide Isolated

- **Bulk isolated**
  - Process more expensive than oxide isolated
  - Process integration scheme has process control challenges
  - Bulk starting wafer with Channel Stop Implants

- **First introduced at 22nm**
  - Challenging bring up
  - First generation performance lacking
  - Expect second generation improvement

- **Foundries following 22nm lead for 14/16nm**
  - Major foundry FINFET introduction will be bulk isolated
  - 10nm needs to address some of the bulk challenges

- **Oxide isolated**
  - Isolation process simpler less expensive
  - Many control issues improved over bulk isolated FinFet
  - SOI starting wafer

- **IBM choice for internal clients**
  - Lower risk
  - Better power/performance

- **IBM 10nm JDA investigating both options**
  - IBM internal 14/10nm is SOI FINFETs
### SOI - Bulk FinFET Comparison

<table>
<thead>
<tr>
<th>Metric</th>
<th>Comparative Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>History Effect</td>
<td>No floating body in either: timing like Bulk planar CMOS</td>
</tr>
<tr>
<td>Isolation</td>
<td><strong>Biggest challenge for bulk FinFET.</strong></td>
</tr>
<tr>
<td></td>
<td>Capacitance/leakage tradeoff.</td>
</tr>
<tr>
<td>Variability</td>
<td>Height control very challenging in bulk fin.</td>
</tr>
<tr>
<td></td>
<td>Isolation doping requirement also adds within-fin nonuniformity.</td>
</tr>
<tr>
<td>Analog FETs</td>
<td>No body contact in either. SOI better due to uniform fin doping.</td>
</tr>
<tr>
<td>Self-heating</td>
<td>Worse in SOI FinFET – minor consideration for most applications. High duty factor circuits may suffer up to 5% drive current penalty.</td>
</tr>
<tr>
<td>Passives</td>
<td>Bulk FinFET can more easily introduce bulk planar passives. SOI FinFET enables planar passives with superior isolation properties.</td>
</tr>
</tbody>
</table>

- **FUNDAMENTALLY** the same – design for both not a problem.
- **SIGNIFICANT** issues in manufacturing – will be addressed by future generation dielectric isolation or other scheme.
Bulk FINFET Challenges

1. Fin height and shape control issues
2. Capacitance from gate to substrate
3. Channel leakage into the page through the bulk Silicon
4. Channel stop implant impacts device performance and Vmin

- **Bulk isolated**
  - Process more expensive than oxide isolated
  - Many process control challenges

- **Bulk challenges**
  - Process control and metrology issues
    - Final fin height the result of multiple un-landed etch steps
    - Fin taper critical: too little = defects, too much = bad device
    - Metrology issues with measuring fin height/taper
  - Many process turns needed to get things right

- **Device challenges**
  - Channel doping and fin taper degrade device
  - Top half of the fin is narrow, with little doping (see chart)
  - Bottom half of the fin is wide, with channel stop doping
  - Multiple steps with direct impact on the device causing variability

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**Tale of two fins: Top fin good, bottom fin bad**

**Superior SCE**
- Smaller fin width
- Better gate control
- Better device
  - DIBL = 45mV/V
  - Ssat = 68mV/d
  - Vt1n = 210mV

**Inferior SCE**
- Wider fin
- Channel doping
- Poor device
  - DIBL = 190mV/V
  - Ssat = 85mV/d
  - Vt1n = 370mV

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Junction-isolated FinFET Tradeoffs

S/D Isolation Methods

- **High Doping**
  - ✔️ minimizes Cgate
  - ✗ high leakage floor
  - ➔ H/S applications

- **Deep Gate**
  -✔️ low leakage floor
  - ✗ Cgate penalty
  - ➔ L/P applications

**Diagrams**

- **X_{OD}**
- **H_{Active Fin}**
- **H_{Parasitic Fin}**

**Figure Notes**

- Leakage floor
- BTBT
- Doping (1/cm³)
- SOI FinFET
- L/P bulk fin
- H/S bulk fin

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SOI vs Junction-isolated FinFETs

- $V_{DD}$ Range is modulated by isolation design
- High channel doping increases RDFs (AVT) $\rightarrow$ Higher Vmin for SRAM.
- High channel doping Increases $E_{OX}$ for given $V_T$ $\rightarrow$ Lower Vmax (BTI and TDDB).
- High AVT also increases Die Iddq for given Ioff $\rightarrow$ Increased product leakage spec.
14nm SOI FINFETs: Significantly better at low voltage!

- Fully depleted devices show improved low voltage operation
- Lower Voltage $\rightarrow$ Lower Power (at const. frequency)

![Graph showing PPG Performance Vs. Vdd](image)
Lower doping → improved AVT → improved SRAM Vmin
Early SRAM Vdd/Vcs SRAM schmoos confirm these predictions (see plot below)
Lower Vmin → lower power operation
14nm SOI FINFETs: Better Thick oxide devices!

AVT improvement even more dramatic on Thick oxide devices

eDRAM data supports the claim
SOI eDRAM Scalability to 14nm

- eDRAM continues to scale with Logic
- Innovations enabling continued scaling include:
  - High-k Trench capacitor
  - N-epi plate
  - FinFET transfer device
- Scaling increases leverage over SRAM
  - Trend expected to continue
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Gate Patterning: SIT PC with WIMPY Support

- Depending on product application, a mix of nominal device and WIMPY device with slightly larger gate length than nominal is needed
- Larger gate length gives lower leakage and variability
- Sidewall Image Transfer (SIT) patterning by itself can only produce one gate CD
- Additional processing steps is needed to enable variable CD

WIMPY process developed to enable 3nm gate CD modulation
Process innovations in SAC RIE and SAC cap formation
Power reduction for 10nm platform

- Relative to 20nm planar technology
- For nominal scaled circuit
  - 0.85X Cload
  - 2.5X Rload

![Realistically-Loaded RVT PPG comparison, TT, 25 C](image-url)
Hardware in line with expectations:

- Functional FETs
  (no punchthrough!)
- Working Ring Oscillators!
Innovations for Cu BEOL for 48nm Pitch (10nm node)

i. Full sacrificial hardmask removal (SACHM) for most metallization-friendly profiles

POR Stack
- Reentrant profiles
- Higher aspect ratio
  ➔ **Defective metallization**

SACHM Stack
- Innovative HardMask and Integration Scheme
- Smallest aspect ratio
- Improved profiles
  ➔ **Void-free metallization**

**Metallization defectivity eliminated**

- EM improved
- TDDB improved
Innovations for Cu BEOL for 48nm Pitch (10nm node)

i. Full sacrificial hardmask removal (SACHM) for most metallization-friendly profiles

- POR Stack
  - Reentrant profiles
  - Higher aspect ratio
  → Defective metallization

- SACHM Stack
  - Innovative HardMask and Integration Scheme
  - Smallest aspect ratio
  - Improved profiles
  → Void-free metallization

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ii. Metal liner and metal cap for reliability extendibility

- EM improved
- TDDB improved

- EM shutdown with new liner and cap

- No Fails

Alternative integration and materials enables void-free dual damasene metallization @ 10 nm node

Selective Metal Cap

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SOI FINFET Scalable to 7nm

- EUV
- Oxide Isolation
- Self-aligned contacts
- Extended Lkg range
- Strained fin
- Density/performance scaling

14nm

Oxide Isolation
- Extended Leakage range
- 2nd pair of work functions
- Self-aligned contacts
- Strained fin

10nm

7nm
3rd generation of FINFET

1st Generation EUV Lithography

Aggressive FIN pitch scaling
  - DSA evaluation

Challenges:
  - Density scaling compared with 10nm
  - Advanced patterning to enable aggressive FIN Pitch scaling
  - Channel material innovation for performance boost
  - MOL and BEOL Via resistances
Look ahead: 7nm Top challenges

<table>
<thead>
<tr>
<th>Top challenges</th>
<th>Focus items</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MOL contact resistance</strong></td>
<td>☐ Material solutions: Dual silicide or MIS contact</td>
</tr>
<tr>
<td><strong>Transport</strong></td>
<td>☐ Alternate channel material: non Si based</td>
</tr>
<tr>
<td><strong>Scalability</strong></td>
<td>1. Gate-stack</td>
</tr>
<tr>
<td></td>
<td>2. Extreme Dfin scaling</td>
</tr>
<tr>
<td><strong>Junction</strong></td>
<td>☐ Alternate doping techniques</td>
</tr>
<tr>
<td><strong>Isolation</strong></td>
<td>☐ Integration with channel material innovation</td>
</tr>
<tr>
<td><strong>Spacer</strong></td>
<td>1. Ultra low-K spacer (k&lt;5) with epi optimization</td>
</tr>
<tr>
<td></td>
<td>2. Spacer variation controls</td>
</tr>
<tr>
<td><strong>BEOL resistance</strong></td>
<td>☐ Innovation of material solutions</td>
</tr>
</tbody>
</table>
### The BIG challenge at 7nm: EUV Introduction!

<table>
<thead>
<tr>
<th>Immersion (ArF)</th>
<th>EUV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Water in Scanner</td>
<td>High Vacuum</td>
</tr>
<tr>
<td>Materials Interactions</td>
<td>New Wavelength (13.5nm)</td>
</tr>
<tr>
<td>Hyper-NA (&gt;1)</td>
<td>Reflective Optics</td>
</tr>
<tr>
<td>Same Wavelength</td>
<td>New Mask</td>
</tr>
<tr>
<td>Same Masks</td>
<td>No Pellicle</td>
</tr>
<tr>
<td>Same Resists</td>
<td>New Resists</td>
</tr>
</tbody>
</table>

- Immersion presented many challenges, but many elements ported from dry ArF
- **EUV is a significantly more challenging endeavor**, requiring more innovative comprehensive solutions
Collaborative development and integration of these technology elements are required to bring EUV Lithography to maturation.

- Alliance Checkpoint for EUV Maturity is 1Q14
EUV Light Source Generation

1. Liquid Sn droplets
2. Pre pulse (shaping)
3. Droplet shape
4. Main pulse (plasma)
5. Plasma and Ejecta
6. EUV light collection
IBM is investing in EUVL

- **Albany’s NFX building will house:**
  - next generation exposure tools
  - mask tools for clean/inspect/repair

- **Huge capital investment in the “EUV Center of Excellence”**
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Industry Migration to Fully Depleted Devices at full steam!!

FINFETs are the basis for technology evolution through the 7nm node
- FINFETs on SOI provide a significant value proposition

Key Upcoming Technology Challenges:
- Device uniformity and Variability control
- EUV migration is imminent (7nm?)
- Materials Innovation → Gate stack scaling and Interconnect reliability / parasitics

Acknowledgments: