

The University of Tokyo, the SOI Consortium, and Soitec are organizing a one day workshop at the Komaba Research Campus (http://www.iis.u-tokyo.ac.jp/access_e/access_e.html) of the University of Tokyo on Saturday the 25th of September 2010 following the SSDM Conference focusing on the FDSOI ecosystem readiness. This workshop is co-organized by Dr. Ishimaru from Toshiba, Dr. Wakabayashi from Sony, Prof. Hiramoto from Tokyo University, Dr. Mogami from Selete, Dr. Fukuma from the Semiconductor Industry Research Institute Japan, Dr. Mazure and Mrs. B.-Y. Nguyen from Soitec, and Dr. Mendez from the SOI Consortium.

Planar FDSOI technology offers today performance gain at very low power consumption in addition to a Vt variability reduction by 50-60% compared to bulk based processes. FDSOI technology enables low Vdd operation for logic and high density SRAM cells at sub-0.6V Vdd regime with excellent SNM and minimum cell size.

Complementing the technical papers and short courses presented during the SSDM conference, the workshop will be devoted to SRAM scaling, design porting from bulk to FDSOI, design flow specificities for FDSOI compared to bulk, BSIM models, power-performance analysis, EDA infrastructure and technology platforms in development. The workshop provides a comprehensive review of the current state of the overall ecosystem presented by renowned experts in the field.

The advanced program is:

- 9:00 Introduction and Welcome (Prof. Toshiro Hiramoto, University of Tokyo)
- 9:10 Market opportunities for sub-0.6V and FD ecosystem (Dr. Horacio Mendez, SOI Consortium)
- 9:30 FDSOI technology (Dr. Bruce Doris, IBM)
- 10:00 Improved SRAM with lowest Vt variability (Prof. Tsu Jae King, Berkeley)
- 10:30 Coffee break

- 11:00 Design enablement and multi wafer project opportunity (Dr. Carlo Reita, Leti-CEA)
- 11:30 FDSOI Power-Performance-Area analysis, Analog and RF (Dr. Fred Boeuf, ST)
- 12:00 Design flow comparison bulk vs. FDSOI (Dr. Jean Luc Pelloie, ARM)
- 12:30 Lunch

- 13:50 Simplified methodology for early SOC architecture analysis (Dr. Diederik Verkest, IMEC)
- 14:20 BSIM SOI and BSIM Multi Gate readiness for FDSOI (tbd, Berkeley)
- 14:50 Problems to be solved for 22/20nm mobile and consumer (tbd, Fabless or Foundry)
- 15:20 Hybrid FDSOI/Bulk integration (Dr. Nobuyuki Sugii, Hitachi)
- 15:50 Coffee Break

- 16:10 HiSIM-SOI readiness (Prof. Shuhei Amakawa, University of Hiroshima)
- 16:40 LSI Industry requirements for consumer (tbd, RENESAS ELECTRIC)
- 17:00 Ultra thin silicon SOI readiness (Olivier Bonnin, Soitec)
- 17:20 Industry requirements for mobile (tbd, SONY)
- 17:40 Closing remarks (Dr. Kazunari Ishimaru, Toshiba)
- 18:00 - 21:00. Reception

The workshop starts at 9:00am and finishes at 6:00pm in the Convention Hall of the Komaba Research Campus of the University of Tokyo. In order to provide time for networking and discussions with the speakers, there will be a reception after the workshop.

The goal of this workshop is to give the highest exposure to FDSOI ecosystem readiness in the areas of technology, modeling, design and EDA. It offers a forum to fabless and IDMs to discuss the needs of SOC ICs for mobile and consumer applications. In addition to SSDM participants there will be an invitation list targeting industry representatives, opinion leaders, decision makers. Goal is to create an expert and business environment for fruitful exchange, for discussions on the potential of the fully depleted IC architecture for mobile and consumer targeting 22nm and beyond.

Registration is free.

Please send your registration to: nicolas.daval@soitec.fr or makoto.yoshimi@soitec.com

We strongly encourage you to participate in the workshop and contribute to the advancement of FDSOI ecosystem with your questions and comments.

We are looking forward to seeing you at the FDSOI Workshop on September 25th, at 9am.

Prof. Toshiro Hiramoto
Professor
University of Tokyo

Horacio Mendez
Executive Director
SOI Consortium

Dr. Carlos Mazure
CTO
Soitec