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## Silicon On Insulator and the future

SOI increases performance per watt, enables designers to reduce supply voltage and power dissipation significantly and demonstrates very important user benefits in a number of highly visible applications (Playstation, Wii, Xbox 360, PowerPC, Opteron...) as well as in many other systems. What limits or delays SOI deployment into many more applications, is a series of outdated misperceptions or rumor-based concerns in executives' and designers' minds. A series of articles will address the most "prominent" of these concerns, starting with "**De-Myth-tifying the SOI Floating Body Effect**".

## What are Floating bodies?

The Floating Body regions of PD-SOI devices are unique to Partially Depleted SOI transistors because of the BOX layer separating the transistor devices from the substrate or bulk wafer material. The inherent advantage that this Floating Body or "tank" region brings to designers is that this region can store charge, which in turn creates a modified switching threshold point. This modified threshold moves up and down slightly due to changes in the stored charge, which help to speed up switching performance. A slice view of the PD-SOI devices is shown in *Figure 1*.

Figure 1. A side view of n-channel and p-channel SOI devices with Floating Bodies.

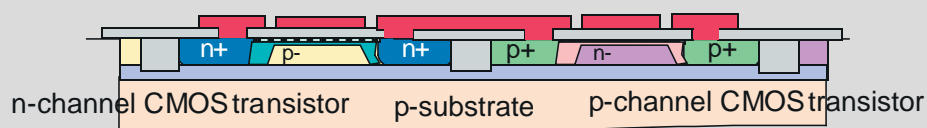
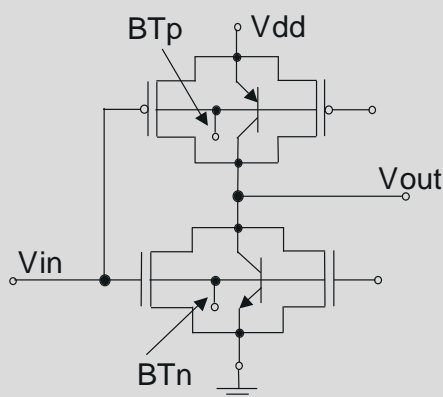


Figure 2. A Floating Body PD-SOI Inverter circuit.

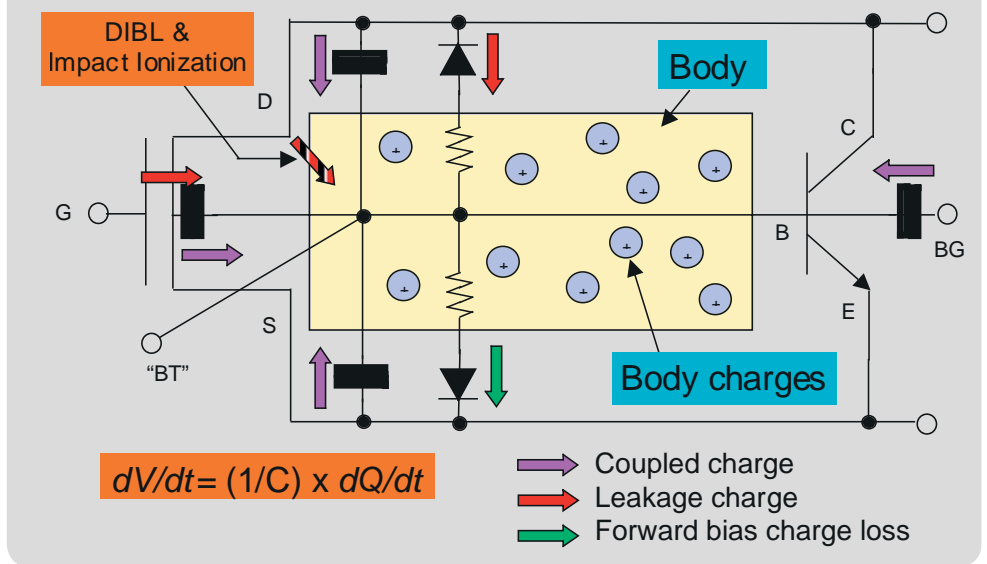


The basic mechanism that causes the variation in threshold for the PD-SOI circuits can be shown for the inverter circuit shown in *Figure 2*. Note that this Figure shows both the parasitic Bipolar transistor that is a part of the CMOS transistor and also shows the Back Gate terminal as an additional control node for the transistor. In our analysis here we will not focus on the Back Gate since it is most commonly grounded through the substrate. It becomes important to see these various pieces of the basic CMOS transistor in order to explain the mechanism by which the Floating Body region accumulates and dissipates charge. In fact, it is this very concept which introduces the benefits of the Floating Body in SOI designs. It should be noted that there are small differences between the n-channel and the p-channel transistor thresholds regardless of whether these devices are created in bulk or SOI technologies. And so designers are already dealing with some "threshold" issues even in bulk technology. The only additional issue that must be accounted for in SOI devices is the additional variation that occurs due to the variable amount of charge in the Floating Body region.

## The Floating body charge model

Although *Figure 2* above does represent the basic inverter circuit, it does not show the mechanism by which charge comes and goes from the Floating Body region. *Figure 3* does show the various ways in which charge is transferred in and out of the FB region for the n-channel device. Note that charge accumulation is due to both leakage currents and coupled charge, and that charge loss or dissipation is due to forward biased current and also coupled charge. These mechanisms will be referred to in the following sections.

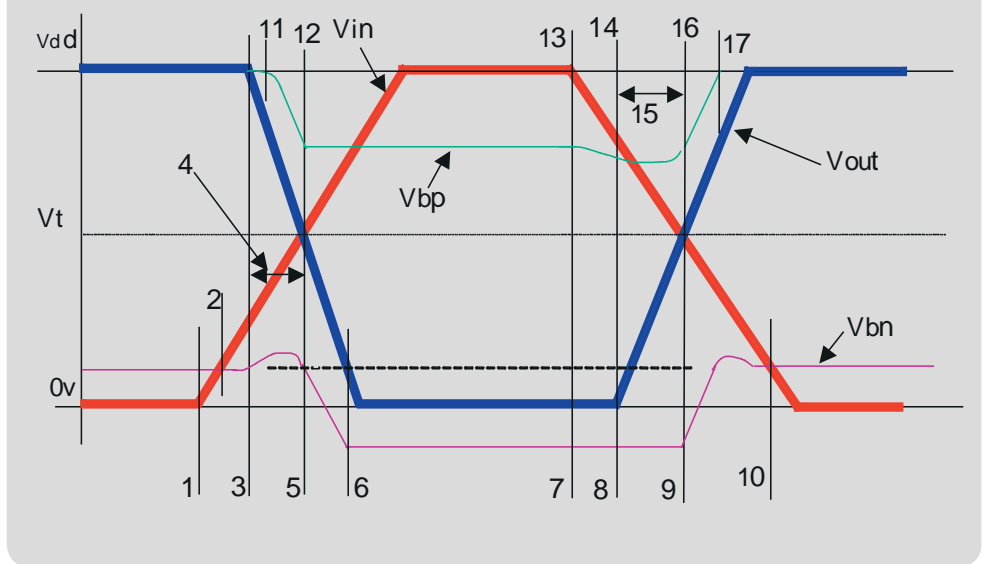
Figure 3. A PD-SOI n-channel schematic showing charging and discharging paths.



### How much threshold variation is there in an SOI device?

The waveforms shown in Figure 4 display the input and output waveforms and the voltage variation present in the Floating Body regions. As you can see, the changes in voltages in the FB regions are much less than the amplitude of either the input or output signal swing. The edges are stretched out horizontally so that the exact mechanism for each change can be clearly identified using the numbers shown in Figure 4.

Figure 4. Switching Waveforms for PD-SOI inverter showing Body Voltages.



It is important to note that the causes of the body voltage variations are primarily due to the charge coupled to and from the Body regions by the capacitors surrounding the body regions, and these are shown in Figure 3 for the n-channel device. There are three basic types of capacitors that control this charge: the Gate Oxide capacitor, the BOX capacitor, and the transistor source and drain capacitors. In a typical PD-SOI circuit, the BOX capacitor does not play much of a role because of the thickness of the BOX region and also because the substrate is often tied to ground and therefore does not provide a large coupled charge. Ideally the substrate is NOT switching constantly and so charge coupling due to fast edge changes is not an issue. But the Gate oxide and the source and drain capacitances (created by the junction depletion regions), provide direct coupling from the Gate and source/drain regions to the Body.

## What causes the body voltage changes shown in Figure 4?

In an ideal world, if the rising and falling input and output signal edges would be step functions, transitions through the threshold regions of a device such as the inverter would not be of much concern since the point in time when the edges passed through the device threshold would be exactly when the edge began to switch. But in the real world, edges are not step functions and so it makes a difference how long it takes a rising or falling edge to actually reach the device threshold. For our initial discussion, we will assume that the device threshold occurs exactly in the middle of the V<sub>DD</sub> to Ground swing as shown in Figure 4. Once we understand the mechanism for the Body voltage changes, we can then account for the fact that actual thresholds are slightly higher or lower than the ideal case of Figure 4.

Figure 4 displays a sequence of numbers from 1 to 17 to allow us to explain exactly what is happening at each of these 17 points that affects the voltages in the body regions. If we use the text below for each of the numbers while referring to Figure 4, we can understand WHY each voltage change occurs in both the n-channel body region and the p-channel body region. As you will note, the fundamental mechanism has to do with the coupling to and from the Gate and the Source and Drain regions of the circuit. Keep in mind also that the voltage in the Body region MUST obey the basic principle that:

$$V = Q/C$$

*So let's take each point in figure 4 and explain it "by the numbers":*

*Input voltage: LOW to HIGH (n-channel initially off)*

1. Input starts to rise (Static Body voltage due to forward and reverse junction currents)
2. Input voltage rises to value of static n-channel Body voltage
3. n-channel Body voltage starts to rise coupled to Gate input
4. Output starts to fall ( $C_{GB} \sim$  cancels  $C_{DB}$  coupling)
5.  $V_{in} = V_{out} = V_{th}$ ; n-channel Body voltage starts to fall through Drain coupling with channel "on" to block Gate to Body coupling
6. Output voltage falls to reach original n-channel Body voltage; n-channel Body voltage stops following output

*Input voltage: HIGH to LOW (n-channel initially on)*

7. Input voltage starts to fall (n-channel body doesn't follow since "on" channel blocks coupling from Gate)
8. Output voltage starts to rise
9.  $V_{in} = V_{out} = V_{th}$ ; n-channel Body voltage starts to rise through coupling to output
10. Output reaches original n-channel Body voltage; n-channel Body voltage stops rising

*Input voltage: LOW to HIGH (p-channel initially on)*

11. p-channel Body voltage starts to fall when output starts to fall through coupling to output (doesn't start sooner because p-channel is "on" which blocks coupling to Gate input)
12. p-channel Body voltage stops falling at threshold (where  $V_{in} = V_{out}$ ) when Gate and Drain coupling tend to cancel each other

### *Input voltage: HIGH to LOW (p-channel initially off)*

- 13.** p-channel Body voltage starts to drop due to Gate coupling
- 14.** p-channel Body voltage stops falling as output voltage starts to rise
- 15.** p-channel Body voltage levels off as coupling to Gate and output tend to cancel each other
- 16.**  $V_{in} = V_{out} = V_{th}$ ; p-channel Body voltage starts to rise through coupling to output (p-channel is now on and blocks coupling to Gate voltage)
- 17.** Output reaches original p-channel Body voltage; p-channel Body voltage stops rising

Notice that a couple of key events take place during time periods 4 and 15 that span a period of time instead of being a single point in time. During these periods, the Gate coupling and the Drain coupling are trying to pull the body voltage in opposite directions. Although they are not perfectly equal, the fact that the edge rates are very similar tends to create a situation where there is no appreciable change in body voltage during these times because the two coupling events “fight each other” and cause the body voltage to remain more or less flat. Where this changes is the point in time when the edges reach the threshold point. At the threshold points, the channels are either turned on or off depending on which edge we are looking at.

For the rising edge that occurs first in *Figure 4*, the n-channel was off before the threshold point, allowing both the input and output edges to compete with one another. On the falling edge of the input, the n-channel was on, effectively blocking the coupling from the Gate to the body. But until the output reaches the threshold point, the n-body region does not start to rise because the n-channel is on and conducting. At threshold, the n-channel begins to turn off. The body voltage will follow the output coupling until the channel is off at which time the two edges compete to keep the body voltage more or less flat. Note that for the falling edge, the fact that the input edge begins falling at time 7, and at time 8 the output begins to react to this change, causes the body voltage to begin rising with the output. But until the input reaches threshold, the channel is not off enough to allow the Gate and Drain coupling to react enough to flatten the body voltage.

### *Side effects*

So far we have addressed the basic mechanisms that govern the change in body voltages in the n and p channel transistors. To do this, we assumed that the device threshold was at one point. In reality, the rising and falling threshold points will be slightly different for a number of reasons. First, as we discussed earlier, the thresholds of the n and p channel transistors are different. This effect will show up mainly on the output waveform because when the n-channel transistor is on it pulls the output low and when the p-channel transistor is on it pulls the output high. If they are both on during an overlap period, then the output voltage would tend to “plateau” until one or both transistors dominate the edge direction. Generally this small overlap period is indeed small and may not even be noticeable on the output waveform. But as input edge rates gets slower, the difference in threshold points can become noticeable because the edge reaches the different thresholds at different times. The fact that the n and p channel devices have different threshold points is a fact of life in both bulk and SOI devices. The primary concern for designers is the impact that the Floating Body has on threshold that could impact device performance.

As we noted in the earlier explanation for the points in *Figure 4*, the major issue is when the channels turn on or off. This is what determines whether or not the Gate and Drain edges are canceling the coupling effect of each other or if one of these edges drives a voltage change in the body region. But as both simulations and measured data have shown, even when a maximum variation in body voltage is accounted for, there is no more than a 5-6 % variation in actual device performance specifically due to the Floating Body Effect. And so designers typically perform a worst case analysis by assuming the maximum variation in the device models and run the Static Timing Analysis for the

worst case min/max corners. It is important to do this so that circuits are designed to deal with the worst case scenario. In reality, once the circuit is operating, body voltage swings will be less than the worst case since charge variations in the body do not span the maximum possible range of charge change that would occur if the device were sitting idle for a long period of time allowing charge to dissipate through leakage paths. The threshold variation occurs as a result of the difference between the “first switch” and the “second switch”, which in effect reflects the difference in charge between a quiescent state and a switching state.

And so this brings us to the secondary “side effect” issue which is that of charge leakage. Up until now we have discussed the idea of charge being stored in the body regions. And the voltage changes that occur are controlled by the coupling from the Gate and Drain regions. But as we know, leakage mechanisms do exist in the real world, and so charge in either of the body regions (n-channel or p-channel) can change due to leakage which is a static effect as compared to a dynamic coupling effect. The big advantage that SOI devices have over bulk devices is that the leakage through the trench isolation and the BOX foundation is much much less than leakage that occurs in a bulk device where most points of leakage occurs through large areas of pn junctions. For the SOI devices, having the BOX then tends to stabilize the charge stored in the Floating Body regions. And for the types of switching speeds in today’s products, the actual variation in stored charge will be less than the maximum possible because the devices are not idle long enough to cause appreciable charge leakage. So the major change in threshold voltage is from idle mode to switching mode (usually referred to as the “first switch” and the “second switch” in STA Models), which accounts for this maximum variation in body voltage by assuming the worst case difference between first and second switch values. And so when designers perform the STA corner analysis, they can easily account for the additional performance variation due to the Floating Body voltage impact. This simply requires that proper models are used during design timing analysis.

## *EDA tool impact*

Fortunately one of the areas to be least concerned about in SOI designs is the impact on EDA Tools Flows. Major EDA Tool vendors such as Cadence Design Systems & Synopsys account for all of the effects unique to SOI technology, such as the Floating Body, Self Heating, Body Ties, and so on. And in fact, the tools can also help designers take advantage of library components such as stacked multiple gate cells based on performance requirements to gain even more performance improvements.

## *Summary*

Myths that Floating Body Effects in PD-SOI devices will cause serious performance issues or catastrophic functional problems are based more on lack of understanding of what is happening to body voltages during both startup and operating modes for these devices than on anything else. Once the mechanism of charge variation is understood, and the fact that good models account for the maximum spread of performance variation, designers can then realize that by doing slightly more timing analysis using existing STA procedures they can completely address the concerns that may cause them to hesitate to move to SOI technology.

In fact, once this hurdle is overcome, designers can realize the significant advantages that SOI technology brings to the party, in terms of issues that impact cost such as a reduction in die size, and can move to taking advantage of lower power, a reduction in parasitic components, and reduced leakage, to realize an actual performance improvement of up to 30% - 40% depending upon the function being realized.

As technology pushes the limits even more to deeper sub micron dimensions, it will become increasingly clear that bulk devices that still rely on junctions associated with the substrate will not be able to compete with all of the advances offered by SOI technology, especially below the 50nm node. And in fact, the one item that appeared most threatening to designers, performance variation due to the threshold impact of the body charge, will become an item on the list of advantages offered by Floating

Body PD-SOI. Designers will trust that library models completely incorporate this threshold variation effect into the already existing Design Flows just as these models already account for timing variations due to many other issues.

Ironically, SOI technology brings about the capacity to reduce system level parasitics such as crosstalk and capacitive effects due to long metal runs to the point where performance improvements will far outweigh issues such as threshold variation due to FB charge variations. Add to this the fact that accommodations for both analog and digital portions of a chip can be made to the advantages of both on the same chip, including lack of Latch Up problems, the ability to match transistors in a single Body region, and a reduction in crosstalk noise (critical to analog circuits).

Some really exciting possibilities that can be explored in SOI technology include the use of more differential circuits that can use very small swings to detect state changes. The idea of using symmetry and differential sensing can create an environment where common mode rejection of device variations could be minimized or eliminated when voltage swings significantly reduce the worry of threshold fluctuations. And of course the ability to use smaller signal swings can allow power supply voltages to be reduced having a big impact on dynamic power dissipation.

Some of the factors that actually contribute more to performance variation than the SOI Floating Body are related to issues such as supply voltage variation, Process doping concentration and dimension variations, metal parasitics, and temperature impact on junction voltages and leakage currents. And these factors have to be accounted for in both Bulk and SOI designs. Bulk CMOS technology has experienced some problems with scaling to smaller dimensions with respect to the ability to control leakage currents through regions such as the Gate Oxide. Recent advances in the area of Hi k dielectric metal Gate materials at the Gate terminal in place of Poly Silicon and Silicon Dioxide allow SOI technology to continue to move to smaller dimensions. PD-SOI devices can further take advantage of design capabilities such as transistor stacking for logic components like multiple input NAND and NOR circuits which can save area and reduce the need for metal connections in some of the logic.

## What's next?

In future articles we'll address why and how self-heating impacts SOI, how SOI helps to reduce die area and/or pack more functionality into an SoC, how to take advantage of SOI in I/O design, how to minimize leakage – especially for designs that operate in high temperatures environments.

The above and other SOI topics will be addressed in a series of articles to show why physics speaks for much broader deployment of SOI Technology, we'll also detail why economics strongly suggests the need to rely on SOI Technology to extend the cost benefits of scaling to 22nm and beyond.

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